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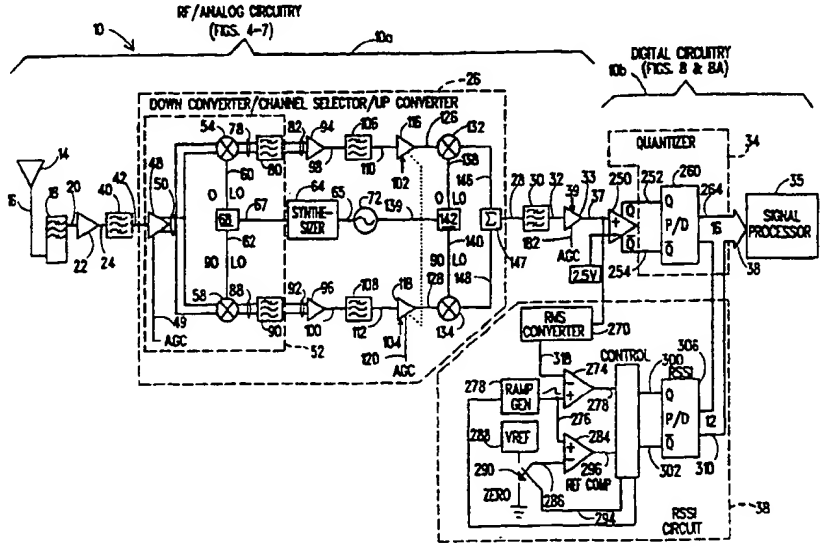

(57) Abstract

A universal receiver (10) for processing RF signals modulated by various analog and digital modulation techniques. The receiver (10) includes a down converter (52) for converting received RF signals to in-phase and quadrature zero IF signals, and active low pass filter (106, 108) for channel selection and an up converter (132, 134) for converting the channel selected in-phase and quadrature zero IF signals to an IF signal. Only moderate system gain is introduced at zero IF in order to avoid increasing any DC offsets. The receiver (10) further includes DC offset compensation circuitry and a period-to-digital (P/D) converter (260) for quantizing the IF signal. A signal processor (35) equalizes and demodulates the IF signal to recover the transmitted signal.

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UNIVERSAL RF RECEIVER

RELATED CASE INFORMATION

This application claims the benefit of U.S. Provisional Application Serial No. 60/001,907, filed August 4, 1995 and U.S. Provisional Application Serial No. 60/010,568, filed January 25, 1996.

FIELD OF THE INVENTION

This invention relates generally to RF receivers and, more particularly, to a highly integrated universal direct conversion receiver for receiving RF signals modulated by any of various analog and digital techniques.

BACKGROUND OF THE INVENTION

Superheterodyne RF receivers which operate by mixing an incoming RF signal with a local oscillator (LO) signal are known. The output of the mixer is an intermediate frequency (IF) signal which is filtered at IF with the use of passive bandpass filters in order to select a particular channel (i.e., frequency) of interest. Such filters generally consist of a resonant element in which the physical properties of the material determine filter characteristics, including filter size. Use of such passive bandpass filters in superheterodyne receivers has precluded size reduction and integration of such receivers.

Another type of receiver that has been considered is the zero IF receiver which, like the superhederodyne receiver, down converts received RF signals. However, instead of down converting to some IF frequency in the manner of a super-heterodyne receiver, zero IF receivers down convert to zero IF (i.e., to the modulating frequency, by removing the carrier frequency). While down conversion to zero IF advantageously permits the use of active filters for purposes of channel selection, zero IF receivers have not been

practical to implement due to the inherent DC offsets which result from the introduction of significant gain at zero IF.

The advent of superheterodyne receivers coincided with the use of analog modulation techniques for RF transmission, such as amplitude modulation (AM) and frequency modulation (FM) techniques. Thus, superheterodyne receivers were developed based on analog modulation standards. With the more recent popularity of wireless transmissions however, including cellular communications, personal communications services and wireless area networks, digital modulation techniques have proliferated. As examples, North America has developed two major standards, including the Code Division Multiple Access (CDMA) IS-95 standard and the North American Digital Cellular (NADC) IS-54 standard. European communities have, in large part, adopted the pan-European digital cellular radio (GSM) standard and Japan has adopted a variation of the NADC IS-54 standard entitled the Personal Digital Cellular (PDC) RCR-27 standard.

SUMMARY OF THE INVENTION

A highly integrated universal RF receiver capable of processing RF signal modulated by various analog and digital modulation techniques is described. The receiver includes a down converter for converting received RF signals to in-phase and quadrature zero IF signals (i.e., baseband signals at the frequency of the modulating signal with the carrier frequency removed). Active channel selection filters pass signals within a desired frequency band and an up converter converts the zero IF signals to an IF signal. Channel selection filtering at zero IF permits the use of readily integratable active filters for this purpose, enabling the receiver to be implemented on one or two application specific integrated circuits (ASICs).

Only moderate gain is introduced at zero IF. Additional gain is introduced to the up converted IF signal. DC offsets

are minimized by avoiding significant gain at zero IF. DC offset compensation circuitry is also provided.

The amplified IF signal is quantized by a Period-to-Digital (P/D) converter which provides a count value signal to a signal processor. In general, the P/D converter is capable of quantizing signals that contain information in the form of phase or frequency modulation (i.e., constant envelope modulation). In such constant envelope modulation schemes, signal information is contained in the zero crossings. The count value signal is representative of the period between consecutive zero crossings of the IF signal and thus, is also representative of the instantaneous frequency of the modulated signal. The P/D converter advantageously uses digital only construction, has low gate complexity and can be fabricated by any of a variety of semiconductor processes.

In one embodiment, a phase comparator compares the amplified IF signal to a reference voltage in order to provide a signal containing zero crossing information to the P/D converter. The phase comparator also serves to amplitude limit the IF signal, thereby eliminating performance degradation due to amplitude fading and the need to otherwise compensate for amplitude fading. Amplitude limiting in this manner is possible due to the use of the P/D converter for equalization, since the P/D converter relies on zero crossing information, as opposed to amplitude information.

The signal processor demodulates the count value signal provided by the P/D converter. Additional functionality of the signal processor includes intersymbol interference (ISI) equalization and additionally, in mobile receiver applications, time dispersion equalization. Clock recovery may also be performed by the signal processor. In one embodiment, the signal processor is a digital signal processor (DSP).

The receiver is compatible with various modulation standards, both analog and digital. In particular, different

modulation standards are accommodated by modifying the bandwidth of an RF input bandpass filter of the receiver, the down converter LO frequency, the IF frequency to which the zero IF signal is up converted and the demodulation technique employed by the signal processor.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing features of this invention, as well as the invention itself, may be more fully understood from the following detailed description of the drawings in which:

Fig. 1 is a block diagram of a universal RF receiver in accordance with the invention;

Fig. 2 is a detailed block diagram of the receiver of Fig. 1;

Fig. 3 is a block diagram of the P/D converter of Fig. 2;

Fig. 4 is a schematic of a first portion of the RF/analog circuitry of the receiver of Fig. 2;

Fig. 5 is a schematic of a second portion of the RF/analog circuitry of the receiver of Fig. 2;

Fig. 6 is a schematic of a third portion of the RF/analog circuitry of the receiver of Fig. 2;

Fig. 7 is a schematic of a fourth portion of the RF/analog circuitry of the receiver of Fig. 2;

Figs. 8 and 8A are a schematic of the digital portion of the receiver of Fig. 2;

Fig. 9 is a graph illustrating peak-to-peak signal levels over the receiver's dynamic range;

Fig. 10 is a functional block diagram of an embodiment of the a signal processor for use in non-mobile receiver applications;

Fig. 11 is a flow diagram of the steps performed by the signal processor of Fig. 10;

Fig. 12 is a functional block diagram of an embodiment of the signal processor for use in mobile receiver applications; and

Fig. 13 is a flow diagram of the steps performed by the signal processor of Fig. 12.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Fig. 1, a universal RF receiver 10 includes an RF bandpass filter (BPF) 18 responsive to transmitted RF signals 16 which are received by an antenna 14. The RF BPF 18 attenuates signals having frequencies outside a particular frequency band of interest.

The filtered output signal 20 of the RF BPF 18 is coupled to a low noise amplifier (LNA) 22 which provides gain to the received signals. The amount of gain provided by the LNA 22 is selected to ensure a satisfactory receiver noise figure (NF), since the LNA 22 is predominantly responsible for establishing the overall system NF. The bandwidth of the LNA is wide enough to pass signals within the frequency band of interest.

A circuit 26 operates to down convert, filter and up convert output signals 24 of the LNA 22. The down conversion is achieved with an image reject mixer (Fig. 2) which converts RF signals to in-phase (I) and quadrature (Q) zero IF signals (i.e., direct conversion). Zero IF signals are baseband signals having the frequency of the modulating signal, with the carrier frequency components removed. The I and Q zero IF signals are then filtered to select a particular channel within the frequency band of interest for reception. In the preferred embodiment, the filter is an active filter. The filtered I and Q zero IF signals are then up converted to respective IF signals and summed to provide an IF output signal 28. In the preferred embodiment, the up conversion is achieved with an image canceling mixer (Fig. 2).

The resulting IF signal 28 is then processed by an IF low pass filter (LPF) 30 which passes the lowest frequency signal components and rejects the odd harmonic components.

The filtered output signal 32 of the IF LPF 30 is further processed by an IF amplifier 33 which provides the additional system gain. The system gain is adjusted over the dynamic range of the receiver, as described in conjunction with Fig. 9 below.

A quantizer 34 is responsive to the IF output signal 37 of the IF amplifier 33 for generating a count value signal 38 for coupling to a signal processor 35. The count value signal 38 is representative of the period between consecutive zero crossings of the IF signal 37 and thus, the instantaneous frequency of the IF signal. In the preferred embodiment, the quantizer 34 is a Period-to-Digital (P/D) converter described in U.S. Patent Nos. 5,159,281, 5,239,273 and 5,272,448, which are assigned to the assignee of the subject application and incorporated herein by reference.

Referring also to Fig. 2, the RF antenna 14 is coupled to the RF BPF 18 which filters out-of-band received signals 16. In one embodiment designed to accommodate GMSK modulated signals and described further below in conjunction with Figs. 4-8A (i.e., the GSM embodiment), the frequency band of interest is between 935Mhz and 960Mhz and the RF BPF 18 has a bandwidth of 25MHz. One suitable type of RF BPF 18 is a duplexer, in which two filters are provided in a single resonant element.

The filtered output signal 20 of the RF BPF 18 is coupled to the LNA 22 for amplification. The bandwidth of the LNA 22 is at least the same as that of the RF BPF 18. The output signal 24 of the LNA 22 may be coupled to an optional additional RF BPF 40 which provides additional out-of-band filtering. Use of the RF BPF 40 may be particularly advantageous in cellular applications.

In the illustrative embodiment, the down converter/channel selector/up converter circuit 26 includes an integrated down converter sub-circuit 52 having an automatic gain control (AGC) amplifier 48 which introduces a selectable gain, such as -3dB or 22dB of gain, to the input

signal 42 in accordance with an AGC signal 49. The AGC amplifier 48 further serves to convert the single-ended input signal 42 to a differential output signal 50. The output signal 50 is coupled to an image reject mixer including an in-phase (I) mixer 54, a quadrature (Q) mixer 58, an I low pass filter (LPF) 80 and a Q LPF 90. Each mixer 54 and 58 receives a respective local oscillator (LO) signal 60 and 62, with the LO signal 62 being 90° out-of-phase with respect to the LO signal 60.

A reference clock oscillator 72, such as a crystal, generates a reference clock signal 65 having a precise frequency, such as 13.0MHz in the illustrative GSM embodiment. A frequency synthesizer 64, such as a phase locked loop (PLL) and a voltage controlled oscillator, converts the reference clock signal 65 into a higher frequency LO signal 67 which is phase-locked to the reference clock signal 65. In particular, the LO signal 67 generated by the frequency synthesizer 64 is matched to the carrier frequency of the RF input signal 16 which, in the GSM embodiment, is between 935MHz and 960MHz. A circuit 68 is responsive to the LO signal 67 for generating the in-phase LO signal 60 and the quadrature LO signal 62 which are thus, phase-locked to the reference clock signal 65.

In order to illustrate the operation of the image reject mixer, consider the case where the differential signal 50 coupled to the mixers 54, 58 is given by $\cos(\omega_c t)$, the I LO signal 60 is given by $\cos(\omega_o t)$ and the Q LO signal 62 is given by $\cos(\omega_o t - 90°)$, where the LO frequency ω_o is equal to the carrier frequency ω_c. The output signal I(t) 78 of I mixer 54 is then given by:

$$I(t) = \cos(\omega_c t) \cdot \cos(\omega_o t) = 1/2\cos(\omega_c + \omega_o)\, t + 1/2\cos(\omega_c - \omega_o)\, t \quad (1)$$

This I(t) signal is then filtered by the LPF 80 which eliminates the summation term. Thus, the $I_f(t)$ output signal 82 of the LPF 80 is given by:

$$I_f(t) = 1/2\cos(\omega_c - \omega_o)t \quad (2)$$

Since the LO frequency ω_0 is matched to the carrier frequency ω_c, the signal $I_f(t)$ can be expressed as the zero IF signal:

$$I_f(t) = 1/2\cos(0)t \quad (3)$$

The output signal Q(t) 88 generated by the Q mixer 58 is given by:

$$\begin{aligned} Q(t) &= \cos(\omega_c t)\cdot\cos(\omega_o t - 90^\circ) \\ &= 1/2\cos(\omega_c t + \omega_o t - 90^\circ) + 1/2\cos(\omega_c t - \omega_o t + 90^\circ) \end{aligned} \quad (4)$$

The Q(t) signal 88 is then filtered by the LPF 90 to generate an output signal $Q_f(t)$ 92 which contains only the frequency difference term as follows:

$$Q_f(t) = 1/2\cos((\omega_c - \omega_o)t + 90^\circ) \quad (5)$$

Again, since the LO frequency ω_0 is matched to the carrier frequency ω_c, the signal $Q_f(t)$ can be expressed as the zero IF signal:

$$Q_f(t) = 1/2\sin(\omega_c - \omega_o)t = 0 \quad (6)$$

Moderate gain may be provided at zero IF in both the I and Q signal paths by respective instrumentation amplifiers 94 and 96. The optional additional linear gain provided by the amplifiers 94, 96 helps to establish the desired overall system NF. However, most of the system gain is not provided at zero IF in order to minimize DC offsets. Additionally, the instrumentation amplifiers 94, 96 convert the respective

differential input signals 82, 92 into single-ended output signals 98, 100, respectively. In the illustrative GSM embodiment, each of the instrumentation amplifiers 94, 96 provides a fixed 6dB of gain.

The single-ended output signals 98, 100 of the instrumentation amplifiers 94, 96, respectively, are coupled to respective active LPFs 106, 108 which are active filters operable to pass the desired frequency spectrum (i.e., channel selection) while attenuating noise and interference outside of the desired signal bandwidth. Since channel selection and interference rejection is performed at zero IF, active LPFs 106, 108 are suitable for providing such functionality. Advantageously, active LPFs 106, 108 are readily integratable. In the illustrative embodiment, each of the LPFs 106, 108 is implemented as an eight pole Bessel filter, as shown and described below in conjunction with Fig. 5. It will be appreciated by those of ordinary skill in the art however, that the LPFs 106, 108 may be provided by any suitable active filter, such as switched capacitor filters. In the GSM embodiment, LPFs 106, 108 provide matched filter response for the receive channel. Additionally, any filter structure which can approximate the required gaussian filter response would suffice for LPFs 106, 108, provided they feature minimal group (phase) delay.

Additional gain is introduced to the output signals 110, 112 of the LPFs 106, 108, respectively, by IF amplifiers 116, 118. The IF amplifiers 116, 118 provide a selectable gain in accordance with an AGC signal 120 in order to establish the total system gain and the overall system NF. For example, in the GSM embodiment, each of the amplifiers provides a gain of 0dB or 20dB.

The amplifiers 116 and 118 are additionally responsive to DC offset compensation circuitry, as indicated by respective DC offset control signals 102, 104. The DC offset compensation circuitry will be described in conjunction with Fig. 5 below. Suffice it to say that the DC offset circuitry

serves to minimize DC offsets at the outputs of the IF amplifiers 116 and 118, such as may be caused by differential DC offsets at the outputs of the image reject mixers 54, 58.

The output signals 126, 128 of the IF amplifiers 116, 118 are up-converted by an image canceling mixer, including an I mixer 132 and a Q mixer 134 responsive to respective LO signals 138, 140. In particular, a circuit 142 is responsive to a divided version 139 of the reference clock signal 65 for generating the in-phase LO signal 138 and the quadrature LO signal 140, which is 90° phase-shifted relative to the signal 138. In the illustrative GSM embodiment, the LO signals 138, 140 have a frequency which meets the Nyquist criterion for the data rate of the transmitted GSM signal or 203.125KHz, where the GSM data rate is equal to 270.833KHz.

In order to illustrate the operation of the up converting mixers 132, 134, consider the case where the single-ended I signal 126 is given by $\cos\omega_m t$, the single-ended Q signal 128 is given by $\cos(\omega_m t-90°)$, the LO signal 138 is given by $\cos(\omega_o t)$ and the LO signal 140 is given by $\cos(\omega_o t-90°)$, where the LO frequency ω_o is equal to the data rate of the transmitted RF signal. In this case, the output signal $I_p(t)$ 146 of mixer 132 is given by:

$$\begin{aligned} I_p(t) &= \cos(\omega_o t)\cdot\cos(\omega_m t) \\ &= 1/2\cos(\omega_o+\omega_m)t + 1/2\cos(\omega_o-\omega_m)t \end{aligned} \qquad (7)$$

and the output signal $Q_p(t)$ 148 of mixer 134 is given by:

$$\begin{aligned} Q_p(t) &= \cos(\omega_o t-90°)\cdot\cos(\omega_m t-90°) \\ &= 1/2\cos(\omega_o t-90°+\omega_m t-90°) + 1/2\cos(\omega_o t-90°-\omega_m t+90°) \\ &= 1/2\cos((\omega_o+\omega_m)t-180°) + 1/2\cos(\omega_o-\omega_m)t \\ &= -1/2\cos(\omega_o+\omega_m)t + 1/2\cos(\omega_o-\omega_m)t \end{aligned} \qquad (8)$$

The $I_p(t)$ and $Q_p(t)$ signals 146 and 148 are then summed by a summation circuit 147 to provide an IF signal S(t) 28 as follows:

$$S(t) = I_p(t) + Q_p(t)$$
$$= 1/2\cos(\omega_o+\omega_m)t + 1/2\cos(\omega_o-\omega_m)t - 1/2\cos(\omega_o+\omega_m)t + 1/2\cos(\omega_o-\omega_m)t$$
$$= \cos(\omega_o-\omega_m)t \quad (9)$$

Consideration of equation (9) reveals that only the lower sideband signal remains, thereby converting the zero IF signals 126 and 128 into an IF signal 28 centered about the LO frequency ω_o.

The IF signal 28 is coupled to the IF LPF 30 which passes the lowest frequency signal components and rejects the odd harmonic response. In the illustrative embodiment described below, the LPF 30 is two cascaded six pole Butterworth filters (Figs. 6 and 7), but may alternatively be implemented with any suitable filter.

The output signal 32 of the LPF 30 is coupled to the IF amplifier 33 which introduces additional gain to the IF signal 32. Amplifier 33 introduces a selectable gain, such as 0dB, 10dB or 20dB, in accordance with an AGC signal 182. Amplifier 33 additionally implements a DC offset correction feature to minimize DC offsets introduced prior to the amplifier inputs in response to a DC offset control signal 39, as will be described below in conjunction with Fig. 7.

The output signal 37 of the amplifier 33 is coupled to a phase comparator 250 and to a Received Signal Strength Indicator (RSSI) circuit 38. The phase comparator 250 configured as a zero crossing detector has a non-inverting input responsive to the output signal 37 of the IF amplifier 33 and an inverting input receiving a reference voltage, such as 2.5 volts. The phase comparator 250 provides a pair of output signals 252, 254 indicative of the zero crossings of the IF signal 37 and which are inverted versions of one another.

More particularly, the phase comparator output signals 252 and 254 are hard amplitude limited pulse trains having transitions at the zero crossings of the IF signal 37. The

hard amplitude limiting of the output signals 252 and 254 reduces amplitude flat fading of the received RF signals, a phenomena which can occur as a mobile receiver moves. In conventional receivers which do not utilize zero crossing detection (i.e., time domain sampling systems utilizing A/D converters as the digitizer), in which the linearity of the processed signals is relied on to determine the phase of the incoming signal, amplitude limiting is not possible; rather, complex equalization techniques have been employed to address amplitude fading. In the present receiver 10 however, it is the zero crossings of the processed signals, rather than their amplitude, that is used by the quantizer 34 to determine the instantaneous frequency of the IF signal, thereby enabling the advantageous technique of hard amplitude limiting to be used to address amplitude fading.

The output signals 252 and 254 of the phase comparator 250 are coupled to the quantizer 34 which is implemented with a P/D converter 260. The P/D converter 260 will be described further in conjunction with Fig. 3 and is the subject of the above incorporated issued U.S. Patents. Additionally, the P/D converter 260 is described in a Numa Technologies data sheet entitled Period to Digital (P/D) Converter NT304 dated 3QTR/94, which is incorporated herein by reference.

The P/D converter 260 integrates the signals 252, 254 with high resolution so as to provide a digital output signal 264 indicative of the instantaneous frequency of the IF signal 37. More particularly, the output of the P/D converter 260 is a sixteen bit count value signal 264 having a value equal to the number of clock cycles which occur between consecutive zero crossings of the IF signal 37. Since frequency is inversely proportional to period, the count value signal 264 can be expressed as:

$$(1/f)/2 \qquad (10)$$

where f is the instantaneous frequency of the IF signal 37. The count value signal 264 of the P/D converter 260 is equalized and demodulated by the signal processor 35, as will be described below in conjunction with Figs. 10-13.

As noted, the output signal 37 of the IF amplifier 33 is further coupled to the RSSI circuit 38. The RSSI circuit 38 shown in Fig. 2 is a linear slope integrating analog-to-digital (A/D) converter, as described in a National Semiconductor Application Note 260 entitled "A 20-Bit (1 ppm) Linear Slope-Integrating A/D Converter" which is incorporated herein by reference. However, it will be appreciated that various A/D converter configurations are suitable for determining received signal strength, such as the successive approximation A/D converter 282 shown in the GSM embodiment below (Figs. 8 and 8A).

The RSSI circuit 38 includes an RMS to DC converter 270 which converts the RMS value of the IF signal 37 to a DC signal 318 for further coupling to the inverting input of a comparator 274. A non-inverting input of the comparator 274 is responsive to a ramp signal 276 generated by a ramp generator 278. The comparator 274 compares the DC signal 318 to the ramp signal 276 and provides an output signal 278 to a control circuit 280, as shown.

The ramp signal 276 is further coupled to a comparator 284 which compares the ramp signal to a reference signal 286. The reference signal 286 is selectively provided by either a reference voltage source 288 or ground in accordance with the position of a switch 290 controlled by the control circuit 280 via a control signal line 294. The output signal 296 of the reference comparator 284 is a reference output signal coupled to the control circuit 280, as shown.

The control circuit 280 provides Q and $\overline{Q}$ output signals 300 and 302, respectively, to a second P/D converter 306. A twelve bit count value signal 310 is provided by the P/D converter 306 to the signal processor 35. With these signal

widths provided by the P/D converter 306, the signal processor 35 is able to calculate the RSSI as follows:

$$\frac{C_{VIN}-C_{ZERO}}{C_{FSREF}-C_{ZERO}} \cdot K\mu V \qquad (11)$$

where C_{VIN} is the count provided by the P/D converter 306 in response to the comparator output signal 278, C_{ZERO} is the count provided by the P/D converter 306 in response to the reference comparator output signal 296 when its inverting input is connected to ground, C_{FSREF} is the count provided by the P/D converter 306 in response to the reference comparator output signal 296 when its inverting input is connected to the reference voltage source 288 and K is a constant, such as 10^7. Note that the P/D converter is available in a sixteen bit output version, as in the case of the quantizer P/D converter 260, or a twelve bit output version, as in the case of the RSSI P/D converter 306.

As should now be apparent, baseband signals are processed from the instrumentation amplifiers 94, 96 through the quantizer 34. This baseband processing portion of the receiver may be fabricated as an ASIC, by either a bipolar, CMOS or BiCMOS process. Although both the RF and baseband receiver portions may be integrated on a single die using a BiCMOS process, isolation considerations may render it desirable to provide separate RF and baseband devices.

Referring also to Fig. 3, a block diagram of an illustrative P/D converter 260 is shown. In general, the P/D converter is capable of quantizing signals that contain information in the form of phase or frequency modulation (i.e., constant envelope modulation), such as Frequency Shift Keying (FSK), Gaussian Minimum Shift Keying (GMSK), Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK) modulation techniques. In such constant envelope modulation schemes, signal information is contained in the zero crossings.

The P/D converter 260 includes a pair of gates 350, 352, each responsive to a respective one of the phase comparator output signals 252 and 254 (Fig. 2) and to a CLK signal 356. Control signals 360 and 362 are further coupled to gates 350 and 352 by a timing and control circuit 370. The control signals 360 and 362 operate to alternatingly enable the gates 350 and 352. The gates 350, 352 are coupled to respective sixteen bit counters 372, 374.

When the input signal 252, 254 to one of the gates 350, 352 is high, the associated counter 372, 374, respectively, advances one count for each cycle of the CLK signal 356. The counters 372 and 374 thus provide respective digital count value signals 376, 378 representative of the period of a half cycle of the IF signal 37 (Fig. 2). The count value signals 376 and 378 are further coupled to respective data latches 380 and 382, as shown.

A FIFO 390 alternatingly receives the latched count value signals from latches 380 and 382 in accordance with enabling control signals 384 and 386 which control the data latches 380 and 382, respectively. The output of the FIFO 390 is in the form of a sixteen bit DATA OUTPUT count value signal 264.

An interface and control circuit 404 provides the control interface to the signal processor 35 (Fig. 2). Asynchronous operation of the P/D converter 260 is accomplished by reading the DATA OUTPUT signal 264 at a rate greater than two times the frequency of the input signals 252, 254. Synchronous operation, on the other hand, is accomplished by using the $\overline{DA}$ output signal 406 of the interface and control circuit 404. A low $\overline{DA}$ signal 406 indicates the availability of data at the output of the FIFO 390.

A $\overline{RESET}$ input signal 408 is applied upon power up in order to ensure proper initialization. In particular, the $\overline{RESET}$ signal, generated by reset circuitry 450 (Fig. 8) causes the

FIFO 390 and counters 372, 374 to be cleared. A $\overline{WR}$ input signal 410, in conjunction with a $\overline{CS0}$ signal 414 and a CS1 418 signal, causes the same action as the $\overline{RESET}$ signal, except that the $\overline{WR}$ reset is issued by the signal processor 35. An $\overline{RD}$ input signal 412, in conjunction with the $\overline{CS0}$ signal 414 and the CS1 signal 418, causes the DATA OUTPUT signal 264 to change from a tri-state condition to enabled. Data is shifted out of the FIFO 390 on the falling edge of the $\overline{RD}$ signal. The $\overline{CS0}$ signal 414 and the CS1 signal 418 are chip select input signals. When the $\overline{CS0}$ signal 414 is low and the CS1 signal 418 is high, these inputs indicate that the control and data lines of the P/D converter 260 are valid and that the operation specified by the $\overline{RD}$ and $\overline{WR}$ inputs should be performed.

Additional circuitry of the P/D converter 260 includes a divider 360 which is responsive to the CLK signal 356 for generating various frequency sub-multiples of the CLK signal, such as four, eight, sixteen, thirty-two and sixty-four at signal lines 392, 394, 396, 398 and 400, respectively. The clock signals 392-400 may be used as a clock source for other devices, such as the signal processor 35.

Referring also to Figs. 4, 5, 6 and 7 RF/analog portions 10a (Fig. 2) of the receiver 10 are shown. In particular, Fig. 4 shows the receiver 10 from the RF input 16 through the instrumentation amplifiers 94, 96, Fig. 5 shows the receiver 10 from the LPFs 106, 108 through the IF amplifiers 116 and 118, Fig. 6 shows the receiver 10 from the up converting mixers 132, 134 partially through the IF LPF 30, and Fig. 7 shows the remainder of the RF/analog portion of the receiver through the IF amplifier 33. Figs. 8 and 8A show the digital portion 10b (Fig. 2) of the receiver. The circuit of Figs. 4-8A represents an embodiment of the receiver adapted for receiving signals in a GSM cellular system (i.e., the GSM embodiment). The modulation technique used in GSM systems is .3Bt Gaussian Minimum Shift Keying (GMSK). Pertinent

parameters of a GSM system are a data rate of 270.833KHz, received signal frequencies between 935.2MHz and 959.8MHz and channel spacing of 200KHz.

With particular reference to Fig. 4, the RF input 16 is coupled to the RF BPF 18, which, in the illustrative embodiment may be of the type sold by Integrated Microwave under the part number 917745. The output signal 20 of the RF BPF 18 is coupled to the LNA 22 which may be of the type sold by Amplifonix under the part number AXO686. The optional RF BPF 40 may be coupled to the output of the LNA 22, as shown.

As noted above, DC offset compensation circuitry compensates for DC offsets at the I and Q IF amplifiers 116, 118 as well as at the IF amplifier 33. The DC offset compensation circuitry associated with the I and Q IF amplifiers 116, 118 operates, generally, by measuring the DC offset during intervals when RF signals 16 are not being received and using this measured DC offset to compensate for the actual DC offset occurring during operating intervals when RF signals 16 are received. More particularly, most digital modulation techniques, including GMSK, utilize Time Division Multiple Access (TDMA) by which RF energy is received in bursts. Because the receiver 10 is not continuously receiving RF signals, the receiver is "powered down" during intervals when no RF signals are received. In particular, the LNA 22 is powered down and the antenna 14 (Fig. 2) is decoupled from the receiver 10.

To accomplish this power down/blocking operation, a switch 36 is coupled between a reference voltage, such as +5 volts, and signal line 24 via a resistor R1, an inductor L1, a capacitor C1 and a capacitor C3, as shown. The switch 36 is responsive to an LNA control signal 41 provided by the digital portion 10b of the receiver (Figs. 8 and 8A) via a connector J1. With this arrangement, when the LNA control signal 41 is low, the switch 36 is closed so as to bias the output of the LNA 22; whereas, when the LNA control signal

41 is high, the switch 36 is open, thereby preventing the output of the LNA 22 from being biased.

The LNA control signal 41 is further coupled to a driver 66 which provides output signals 70, 74 to a switch circuit 84, as shown. The switch circuit 84 is operable to isolate the RF input 16 from down stream portions of the receiver 10. That is, during operating intervals when RF signals are received, the output signals 70, 74 of the driver 66 cause the switch 84 to serially connect its RF1 input to its RFC output. Alternatively however, during operating intervals when RF signals are not being received, the output signals 70, 74 of the driver 66 open the switch 84 so as to decouple the RF1 input from the RFC output. Additionally, RFC is connected to RF2 in order to terminate the impedance matching network comprising C150, L3 and L6 into a 50 ohm terminating impedance connected to RF2 output, thereby decoupling the RF input 16 from down stream portions of the receiver 10.

The RFC output of the switch 84 is coupled to the down conversion sub-circuit 52 (Fig. 2). In particular, the RFC output is coupled to an $\overline{RF}$ input of sub-circuit 52. Recall from Fig. 2 that the sub-circuit 52 includes the AGC amplifier 48, the I and Q down conversion mixers 54 and 58, and the I and Q LPFs 80 and 90, respectively. Thus, the outputs of the sub-circuit 52 are two pairs of differential signal lines 82 and 92, as shown. Signal 82 provides the differential I output of the sub-circuit 52 and signal 92 provides the differential Q output of the sub-circuit 52. In the illustrative embodiment, the down conversion sub-circuit 52 is of the type sold by Temic Telefunken Semiconductors under the part number U2791B and described in a Temic data sheet entitled 1000MHz Quadrature Demodulator U2791B, dated 08.06.1995 and incorporated herein by reference.

The down conversion sub-circuit 52 is additionally responsive to AGC signal 49 for causing the internal AGC amplifier 48 to selectively introduce -3dB or 22dB of gain.

In particular, the AGC signal 49, labelled GC0, is provided by the signal processor 35 (Fig. 8A). The GC0 signal controls a switch Q1 such that, when the GC0 signal is high, the GC pin of the sub-circuit 52 at the collector of switch Q1 is pulled low, causing 22dB of gain to be introduced by the internal AGC amplifier 48. When the GC0 signal is low on the other hand, the GC pin of the sub-circuit 52 is high, causing -3dB of gain to be introduced by the AGC amplifier 48.

As noted above, most digital modulation techniques employ TDMA access. However, the receiver 10 is equally operable in the case of continuous modulation techniques, whereby RF signals are continuously received by the receiver 10. In such continuous applications, the DC offset correction provided by the DC offset circuitry described herein may be enhanced by including optional capacitors C73, C74, C120 and C125. In particular, the AC coupling provided by these capacitors blocks any DC offset at the outputs of the down conversion mixers 54, 58 within sub-circuit 52. However, use of the capacitors C73, C74, C120 and C125 in discontinuous receiver applications may be detrimental to the DC offset, since the resulting RF level shifts generate a DC component which is subject to integration by the capacitors, thereby aggravating any DC offset introduced by the mixers. Thus, in discontinuous receiver applications, capacitor C73, C74, C120 and C125 are jumpered or otherwise removed.

The reference clock oscillator 72 provides the reference clock signal 65 (OSCOUT) having a predetermined frequency. In the GSM embodiment, the reference clock oscillator 72 is a crystal operating at 13.0MHz. The OSCOUT signal 65 is coupled to the frequency synthesizer 64 converts the OSCOUT signal 65 to a signal 67 having a frequency matched to the carrier frequency. More particularly, the synthesizer 64 is responsive to control signals 75 via a connector 73 which set the frequency of the LO signal 67 provided by the synthesizer. The control signals 75 may be provided by any suitable user interface, such as a microprocessor. The down

conversion sub-circuit 52 includes the circuit 68 which provides the in-phase LO signal 60 and the quadrature LO signal 62 to the I and Q mixers, respectively. In the illustrative embodiment, the OSCOUT signal 65 is coupled to the signal processor 35 (Fig. 8A), where it is divided by sixteen to generate an 812.5KHz LO signal 139 for use in up conversion, as will be described.

Downstream of the sub-circuit 52 are the instrumentation amplifiers 94 and 96 which may be of the type sold by Burr-Brown under the part number INA118. In one embodiment, each of the instrumentation amplifiers 94 and 96 introduces a fixed 6dB gain.

Referring also to Fig. 5, the matched LPFs 106, 108 (Fig. 2) are shown. In the illustrated embodiment, the LPFs 106 and 108 are implemented as eight pole Bessel filters, each having four stages 106a, 106b, 106c, 106d and 108a, 108b, 108c, 108d, respectively. Recall that the LPFs 106 and 108 provide matched filtering for channel selection. No additional gain is introduced by the LPFs 106 and 108.

The I and Q frequency selected output signals 110, 112 of the LPFs 106, 108, respectively, are coupled to the inverting input terminals of respective IF amplifiers 116, 118, as shown. The IF amplifiers 116 and 118 have a selectable gain associated therewith. In the illustrative embodiment, amplifiers 116, 118 provide either 0dB of gain or 20dB of gain. To this end, each of the amplifiers 116, 118 has a switch circuit 122, 124 coupled in feedback relationship therewith. Switch circuits 122, 124 have an internal switch between the S1 and S2 pins. The AGC signal 120 (Fig. 2), labelled GC1, is generated by the signal processor 35 and controls the switches 122, 124 in order to selectively open and close the respective internal switch between the S1 and S2 pins. In the event that the GC1 signal 120 causes the internal switch of switch circuit 122 to close, then the feedback resistor of amplifier 116 is provided by the parallel combination of resistors R73 and

R87; whereas if the GC1 signal 120 causes the internal switch to open, then the feedback resistor of the amplifier 116 is provided by resistor R87. Similarly, if the GC1 signal 120 causes the internal switch of switch circuit 124 to open, then the feedback resistor of the amplifier 118 is provided by the parallel combination of resistors R58 and R79; whereas, if the GC1 signal 120 causes the internal switch to open, then the feedback resistor of the amplifier 118 is provided by resistor R79. In the illustrative embodiment, when the GC1 signal is high, each of the amplifiers 116, 118 introduces 20dB of gain and, when the GC1 signal is low, each of the amplifiers 116, 118 introduces 0dB of gain.

Recall that in TDMA receiver applications, when RF signals are not received, the LNA 22 is powered down and the RF input 16 blocked from the receiver 10. When the LNA 22 is powered down and the RF input 16 is blocked from downstream portions of the receiver 10, the DC offset compensation circuitry associated with IF amplifiers 116 and 118 is operable to measure the DC offset associated with feeding a signal through the receiver 10. This is achieved by feeding a signal through I and Q inverting operational amplifiers 130, 136 and applying the output of such amplifiers to the non-inverting input of respective sample and hold circuits 150, 152. A sample and hold control signal 151 generated by the signal processor (Fig. 8A) is coupled to the sample and hold circuits 150 and 152 for causing the respective output signals 131, 137 of the inverting amplifiers 130, 136 to be sampled. The output signals 153, 155 of the sample and hold circuits 150, 152 are coupled to the non-inverting inputs of the IF amplifiers 116, 118, respectively, as shown.

With this arrangement, the DC offset attributable to the components of the receiver 10 up stream of the IF amplifiers 116, 118 is measured, inverted and subtracted from the processed IF signals 110, 112. In this way, any such DC

offset appearing at the IF amplifiers 116, 118 is compensated in the respective output signals 126, 128.

Referring also to Fig. 6, the output signals 126 and 128 of the I and Q IF amplifiers 116 and 118 are coupled to unity gain inverting amplifiers 164 and 166. The output signals 168 and 170 of the inverting amplifiers 164 and 166, respectively, are coupled to inputs of a quad FET switch 174, such as the type sold by Maxim under the part number MAX393. The quad FET switch 174 provides the up conversion mixer functionality of mixers 132, 134 (Fig. 2). The switch 174 includes four internal FETs (FET1, FET2, FET3 and FET4), each having a drain coupled to a respective pin D1, D2, D3, D4, a source coupled to a respective pin S1, S2, S3, S4 and a gate coupled to a respective pin IN1, IN2, IN3, IN4.

The switch 174 is further responsive to the LO signals 138, 140. In particular, The LO signals 138 and 140 are generated in response to an LO signal 139 from the signal processor 35 (Fig. 8A) by a flip-flop circuit 142, as shown. In particular, a flip-flop 142a divides the signal 139 by four and phase-shifts the signal by 90° to provide the LO signal 140 to the Q mixer 134 (i.e., to the IN3 and IN4 inputs to switch 174) and a flip-flop 142b divides the signal 139 by four to provide the LO signal 138 to the I mixer 132 (i.e., to the IN1 and IN2 inputs to switch 174). Since the LO signal 139 has a frequency of 812.5KHz in the GSM embodiment, the LO signals 138, 140 have a frequency of 203.125KHz to satisfy the minimum Nyquist frequency required for the data rate of the transmitted GSM signals.

Considering the I channel for example, input signal 126 is coupled to the drain of FET1 and 90° phase-shifted signal 168 is coupled to the drain of FET2. The sources of FET1 and FET2 are externally coupled together at the S1 and S2 pins, as shown. The gates of FET1 and FET2 are likewise externally coupled together at the IN1 and IN2 pins. The Q channel is similarly mixed by a pair of FET switches, FET3 and FET4, one of which, FET3, has a drain terminal coupled to signal 128

and the second of which, FET4, has a drain terminal coupled to 90° phase-shifted signal 170. The sources of FET3 and FET4 are commonly connected external to the switch 174 at pins S3 and S4. The gate terminals of FET3 and FET4 are likewise commonly connected at the IN3 and IN4 pins, as shown.

The I output signal 146 of the up conversion switch 174 is coupled to an inverting input terminal of a summing amplifier 176. The Q output signal 148 of the switch 174 is likewise coupled to the inverting input of the summing amplifier 176. The output signal 28 of the summing amplifier 176 is thus, the sum of the signals 146 and 148 and, in particular, is given by equation (9) above.

The summed IF signal 28 is coupled to the LPF 30, as shown. In the illustrative embodiment, the LPF 30 is implemented with two six pole Butterworth filters, four two pole stages of which are shown in Fig. 6 (30a, 30b, 30c and 30d) and the last two two pole stages of which are shown in Fig. 7 (30e and 30f). Each of the operational amplifiers in the Butterworth filter 30 may be of the type sold by Linear Technologies under the part number LT1214, for example.

The output signal 32 of the IF LPF 30 is coupled to the IF amplifier 33 which, in the illustrative embodiment, is implemented in two stages 33a, 33b. The IF amplifiers 33a and 33b are responsive to a AGC signals 182 for selecting the gain to be introduced by such amplifiers. In particular, each of the IF amplifiers 33a and 33b provides 0dB or 10dB of gain. The gain provided by each such amplifier stage is selected by a quad FET switch 180, of the type described above in conjunction with the up conversion mixers, in response to control signals 182. FET1 and FET2 control the gain of the first amplifier stage 33a. Control signals 182 alternatingly actuate FET1 and FET2 such that, at any given time, one of FET1 and FET2 is closed and the other is open. In particular, if FET1 is on (i.e., closed), then feedback resistor R72 is connected between the inverting input and

output of amplifier 33a and if FET2 is closed, then the feedback resistor R55 is connected between the inverting input and output of amplifier 33a. In a similar manner, FET3 and FET4 of switch 180 control the gain of the amplifier stage 33b. Control signals 182 alternatingly control FET3 and FET4 such that only one of such FETs is on at any given time. If FET3 is closed, then feedback resistor R149 is connected between the inverting input and output of amplifier 33b and if FET4 is closed, then the feedback resistor R126 is connected between the inverting input and output of amplifier 33b. In the illustrative embodiment, control signals 182 are provided by signal processor generated GC2 and GC3 signals 181 (Fig. 8A). Specifically, when GC2 and GC3 are both low, stages 33a and 33b introduce 0dB of gain and when GC2 is high and GC3 is low, each of stages 33a and 33b introduces 10dB of gain.

Additional DC offset compensation circuitry is provided for the gain stage 33 by a servo amplifier 200 which compares the output signal 37 of amplifier stage 33b to a reference voltage. The output signal 204 of the servo amplifier 200 is fed back to the non-inverting inputs of the amplifiers 33a and 33b, as shown. With this arrangement, the DC offset associated with the amplifiers 33a, 33b is compensated. In the illustrative embodiment, the servo amplifier 200 is of the type sold by Maxim under the part number MAX400.

The phase comparator 250 receives the IF output signal 37 of the amplifier stage 33b at its non-inverting input and a reference voltage at its inverting input, such as 2.5 volts. The Q and $\overline{Q}$ output signals 252, 254 of the phase comparator 250 are indicative of the zero crossings of the IF signal 37. Phase comparator output signals 252, 254 are coupled to the quantizer 34 (Fig. 8). In the illustrative embodiment, the phase comparator is of the type sold by Maxim under the part number MAX913.

The IF signal 37 is additionally coupled to the RSSI circuit 38, a portion of which is shown in Fig. 7. In

particular, the IF signal 37 is coupled to a 2X inverting amplifier 258, the output of which is coupled to the RMS to DC converter 270. The output signal 262 of the RMS to DC converter 270 is further processed by an operational amplifier 268 which provides an RSSI signal 310 to an A/D converter 282 (Fig. 8).

Referring also to Figs. 8-8A, the digital portion 10b of the receiver 10 is shown to include the quantizer 34, RSSI circuit 38 and signal processor 35. In the GSM embodiment, the RSSI circuit includes a successive approximation A/D converter 282 of the type sold by Maxim under part number MAX153. The output of the A/D converter 282 is an eight bit digital signal 292 representative of the RMS amplitude of the received RF signal. The A/D output signal 292 is coupled to the signal processor 35, as shown. In particular, the signal processor 35 selects between the P/D converter output signal 264 and the A/D converter output signal 292 for receipt. Chip select logic 308 is provided for this purpose.

The Q output signal 252 and the $\overline{Q}$ output signal 254 of the phase comparator 250 are coupled to the P/D converter 260. The CLK signal 356 coupled to the P/D converter is provided by a clock generator 420, such as the illustrated 100MHz crystal oscillator. While the illustrated signal processor 35 is a digital signal processor (DSP), other types of signal processors may be suitable, particularly for non-mobile receiver applications, as described below. The sixteen bit DATA OUTPUT signal 264 and the $\overline{DA}$ signal 406 are coupled from the P/D converter 260 to the DSP 35 and the P/D converter 260 receives the $\overline{CS0}$ signal 414, the CS1 signal 418, the $\overline{RD}$ signal 412, and the $\overline{WR}$ signal 410 from the DSP 35. More particularly, $\overline{WR}$, $\overline{RD}$ and $\overline{DMS}$ output signals of the DSP 35 are buffered by a buffer 484 to provide the $\overline{WR}$, $\overline{RD}$ and $\overline{CS0}$ input signals to the P/D converter 260 which are also coupled to $\overline{WR}$ and $\overline{RD}$ inputs of the A/D converter 282 and to the chip select circuit 308, as shown. Also provided

in the digital portion 10b of the receiver 10 is power up/reset circuitry 450 for the DSP 35. An EPROM 454 stores the code executed by the DSP 35. Upon power up, code stored in the EPROM 454 is read and executed by the DSP 35.

A one bit latch 458 is coupled to the DSP 35. The A0, A1 and A2 control inputs of the latch 458 (collectively labelled 460) receive control signals from the DSP by which one of the eight latch outputs Q0-Q7 is selected for coupling to the latched data input signal 462. In the illustrative embodiment, only seven of the latch outputs Q0, Q1, Q2, Q3, Q4, Q6 and Q7 are used. In particular, latch output Q0 provides the GC0 signal 49, latch output Q1 provides the GC1 signal 120, latch output Q2 provides the GC2 signal, latch output Q3 provides the GC3 signal, latch output Q4 provides the LNA control signal 41, latch output Q6 provides the sample and hold control signal 151 and latch output Q7 provides the receiver data output signal 470. Enable circuitry 464 provides an enable signal $\overline{E}$ to the one bit latch 458. The GC2 and GC3 signals together (labelled 181) provide gain control signals 182 (Fig. 7) for selecting the gain of amplifier stages 33a and 33b, as discussed above.

The receiver data output signal 470 is representative of the transmitted bit and is coupled to a flip-flop 486 and to a clock recovery circuit 488. A divider/clock source 480 divides the frequency of the OSCOUT signal 65 to generate the LO signal 139 for use in up conversion (Fig. 4) and a second signal 490 for use by the clock recovery circuit 488. In the GSM embodiment, the OSCOUT signal 65 is a 13.0MHz signal which is divided by four to generate the signal 490 at 3.25MHz and is divided by sixteen to generate the LO signal 139 at 812.5KHz.

The clock recovery circuit 488 provides a recovered clock signal 482 at the data rate and in-phase with the transmitted RF signals. The recovered clock signal 482 is coupled to DSP 35 and the flip-flop 486, as shown. The flip-flop 486 clocks the receiver data output signal 470 in

accordance with the recovered clock signal 482 in order to provide an RXDATA signal which is representative of the recovered transmitted bit.

The RSSI circuit output 292 is used by the DSP 35 to adjust the overall system gain via the AGC control signals 49, 120 and 182 (Fig. 2). More particularly, in operation, the gain stages provided by the AGC amplifier 48, the IF amplifiers 116 and 118, and the IF amplifier 33 are sequentially "turned off" (i.e., switched to a gain of 0dB), from the rear of the receiver 10 proximal to the signal processor 35, forward toward the antenna 14 as the received signal strength increases.

Referring to Fig. 9, a graph illustrates peak-to-peak signal level over the dynamic range of the receiver 10. Curve 500 illustrates the signal level of a received RF signal. The other curves 502, 504, 506, 508 and 510 represent gain at various stages of the receiver. Specifically, curve 502 represents the gain at the output of the IF amplifier 33, curve 504 represents the gain at the outputs of the IF amplifiers 116 and 118, curve 506 represents the gain at the output of the up converter mixers 132, 134 and curve 508 represents the gain at the output of the down conversion sub-circuit 52.

The steps in each of these curves represent the "turning off" of the particular gain stage as the received signal strength increases. This operation is performed by the signal processor 35 and, specifically, by signals GC0 49, GC1 120, GC2 and GC3 181 (Fig. 8A). Step 512 represents the gain of amplifier stage 33b being switched from 10dB to 0dB when the received signal strength reaches approximately -85dBm, step 514 represents the gain of amplifier stage 33a being switched from 10dB to 0dB when the received signal strength reaches approximately -75dBm, step 516 represents the gain of amplifiers 116 and 118 being switched from 20dB to 0dB when the received signal strength reaches approximately -65dBm and step 518 represents the gain of amplifier stage 48

being switched from 22dB to -3dB when the received signal strength reaches approximately -45dBm. The choice of when to turn off each of the gain stages is based on a compromise of SNR ratio and signal (i.e., gain) compression, as may occur when excessive signal strengths cause the amplifiers to saturate.

The signal processor 35 demodulates and equalizes the output 264 of the P/D converter 260. Recall that amplitude fading is addressed by the hard amplitude limiting of the phase comparator 250. Thus, the signal processor 35 need not provide equalization to address amplitude fading. Intersymbol interference (ISI) is a phenomena which is introduced deliberately in GSM systems, by the modulator at the transmitter and is produced by each bit of energy being spread over several bit periods, both before and after the currently transmitted bit. This energy spreading is the result of the impulse response of the Gaussian filter at the modulator. The equalizer of the signal processor 35 addresses ISI in order to prevent degradation in the bit error rate (BER) caused by a reduction in the SNR of the receiver. In the illustrative GSM embodiment, ISI equalization is achieved with a decision-feedback equalization (DFE) approach.

Referring to Fig. 10, a functional block diagram of an embodiment of the signal processor 35 for use in non-mobile receiver applications is shown. Demodulation, or signal detection, is achieved with a one-bit differential detector. To this end, the P/D converter 260 provides the count value signal 264 representative of the period between consecutive zero crossings of the IF signal 37 to an integrator 580 of the signal processor 35. The count value signal 264 is integrated over a one bit time interval T_b as provided to the integrator by a signal 584.

ISI equalization is performed by summing the integrated signal 581 with a DFE signal 583 generated in a manner described below. A data slicer 586 determines whether the

summation signal 585 represents the transmission of a one or a zero over the bit time T_b. The output signal 587 of the data slicer 586 represents the recovered, transmitted bit.

For purposes of linearization, a scale factor α is determined in accordance with whether the output signal 587 is a one or zero. That is, the P/D count value signal generated in response to a mark (logic 1) or a space (logic 0) condition at the modulator (i.e., transmitter) has a non-linear transfer function due to the 1/f or period measurement. For example, in the case where the center IF frequency is approximately 203KHz corresponding to a P/D count of approximately 246, a +67KHz deviation equals an IF frequency of 270KHz and a P/D count value of approximately 184, whereas a -67KHz deviation at the transmitter results in an IF frequency of 135KHz and a P/D count value of approximately 369. In one embodiment, if the transmitted bit is a one, then α is set to -0.67 and, if the transmitted bit is a zero, then α is set to +1.

After a one bit delay 588, the scale factor α is set equal to the previous scale factor value α_{-1}. The previous scale factor α_{-1} is then summed with a DFE constant ϵ 592 by a multiplier 594 to provide the DFE signal 583. The DFE constant ϵ is derived from the transfer ratio of the 1/f P/D process (i.e., the non-linear transfer function). The ISI equalization provided by multiplying the scale factor α_{-1} and the DFE constant ϵ implements a feedback filter 596, which may be referred to as a postcursor equalizer. As such, the feedback filter 596 eliminates the postcursor portion of the ISI (i.e., the interference from past data symbols).

Referring also to Fig. 11, a flow diagram of steps performed by the signal processor of Fig. 10 for demodulation and ISI equalization is shown. The signal processor 35 demodulates received signals by integrating the difference between a currently detected P/D count value signal and a previously detected P/D count value signal over a single bit time. To this end, the signal processor 35 waits for an

interrupt IRQ2 to occur in step 600. Interrupt IRQ2 is generated by the $\overline{DA}$ output signal 406 of the P/D converter 260 at each detected zero crossing.

In step 604, a timer is read to determine the time ET_2 that has lapsed since a prior IRQ2 interrupt was received and the time ET_2 stored. Also in step 604, the timer is loaded with a count of 100 and restarted. Note that in the illustrative embodiment, one bit time is equal to 80 machine cycles, so the timer is loaded with a value greater than one bit time.

The most recently computed difference value d(x) is stored as a previous difference value $d(x)_{-1}$ in step 608. In a subsequent step 612, the current count value signal 264 from the P/D converter 260 (i.e., N) is stored as a previous count value N_{-1}. The current count value N is then provided by the count value signal 264 from the P/D converter 260 in step 616.

Steps 620-648 collectively correspond to the operation of the integrator 580 in Fig. 10. In step 620, the difference value d(x) is calculated by subtracting 246 from the value N. An intermediate integrator value f(x)' is then calculated in step 624 by multiplying the previous difference value $d(x)_{-1}$ by the timer value ET_2. The intermediate integrator value f(x)' is then updated in step 628 by incrementing the intermediate integrator value f(x)' by a previous intermediate integrator value $f(x)'_{-1}$. In step 632, the intermediate integrator value f(x)' is stored as the previous intermediate integrator value $f(x)'_{-1}$. Note that the Mask Off IRQ0 box 634 indicates that the series of sequential steps 604 through 632 is fully executed once entered.

The signal processor 35 then idles in step 636 and waits for a subsequent interrupt IRQ0 in step 640. Interrupt IRQ0 is provided by the 270.833Khz recovered clock signal 482 (Fig. 8A). Once an IRQ0 interrupt is received, step 644 is performed in which the timer is again read and the lapsed

time ET_0 since the prior IRQ0 interrupt stored. The timer is also loaded with a count of 100 and restarted.

Thereafter, in step 648, the integrator value f(x) is updated by adding the intermediate integrator value f(x)' to the product of the difference value d(x) and the timer value ET_0. In step 652, the previous intermediate integrator value $f(x)'_{-1}$ is reset to zero. The Mask Off IRQ2 box 654 indicates that sequential steps 640 through 652 are completed once the sequence is entered. In step 656, the integrator value f(x) is stored as the value I.

Step 660 implements the one bit adaptive DFE equalization discussed above in conjunction with Fig. 10 by which the integrated signal 581 (Fig. 10) is summed with the DFE signal 583. In particular, the value I is summed with the product of the DFE constant ϵ and a previous scale factor α_{-1}.

The data slicer 586 of Fig. 10 is implemented in steps 664 and 680. In particular, in step 664, it is determined whether the value I is greater than or equal to zero. In the event that I is greater than or equal to zero, then the transmitted bit is determined to be a zero. Alternatively, if it is determined in step 680 that I is less than zero, then the transmitted bit is determined to be a one.

In the event that the transmitted bit is determined to be a zero, then step 668 is next performed, in which the scale factor α is set to -.67. Alternatively, if it is determined that the transmitted bit is a one, then step 684 is performed in which the scale factor α of set to +1. After steps 668 and 684, step 672 is performed in which the data signal 462 (Fig. 8A) is provided to the one bit latch 458. The previous scale factor α_{-1} is then set to the current scale factor α in step 676, following which the signal processor 35 idles again in step 636.

In mobile receiver applications, in addition to ISI equalization and demodulation, the signal processor 35 additionally equalizes to address time dispersion. Time

dispersion is a phenomena whereby changes in the impulse response of the mobile channel cause an increased BER. To this end, in mobile receiver applications, an adaptive multipath equalization technique is used to address both time dispersion and ISI equalization.

In order to implement adaptive multipath equalization, in mobile receiver applications, it may be desirable to implement the signal processor 35 with a DSP. In non-mobile receiver applications however, the signal processor 35 may be implemented with hardware logic. This is the because the adaptive equalization used to address time dispersion is not necessary, thereby greatly simplifying the functionality of the signal processor 35.

Referring to Fig. 12, a functional block diagram of a signal processor 35 for use in mobile receiver applications is shown to include an adaptive multipath equalization scheme. The P/D converter 260 provides the count value signal 264 representative of the period between consecutive zero crossings of the IF signal to an integrator 702. Integrator 702 integrates the count value signal 264 over a one bit time interval T_b as provided by a signal 704. The integrated signal 708 is processed by a feedforward filter 710. The feedforward filter 710 may be referred to as a precursor equalizer and performs the function of a whitening matched filter. The feedforward filter 710 also equalizes the precursor portion of the ISI (i.e., interference from future data symbols).

The feedforward filter 710 includes a plurality of delay circuits 712_0, 712_1, 712_2, ...712_n and corresponding feedforward coefficients g_0, g_1, g_2, ...g_{n-1}. Each of the coefficients g_0, g_1, g_2, ...g_{n-1} is multiplied in a multiplier 714_0, 714_1, 714_2, ...714_{n-1} by a respective output signal 718_0, 718_1, 718_2, ...718_{n-1} of a corresponding delay circuit 712_0, 712_1, 712_2, ...712_n. The signals 720_0, 720_1, 720_2, ...720_{n-1} provided by multipliers 714_0, 714_1, 714_2, ...714_{n-1} are coupled

to a summation circuit 724 where they are summed with output signals 714_0, 714_1, 714_2, ...714_{n-1} from a feedback filter 750.

The output of the summation circuit 724 is coupled to a data slicer 728 for determination of the transmitted bit at each bit time T_b and to a summation circuit 730. Summation circuit 730, in conjunction with a coefficient adaptation circuit 739 and a stored training sequence code 738, adaptively determines optimum values for the feedforward coefficients g_0, g_1, g_2, g_3...g_{n-1} and feedback DFE coefficients ϵ_0, ϵ_1, ϵ_2, ϵ_3...ϵ_m. The training sequence code 738 is specified by the GSM specification for the received time slot and, in particular, is specified by the 1994 European Telecommunications Standards Institute (ETSI) Standard GSM 05.02 specification which is incorporated herein by reference.

More particularly, every received GSM burst contains 156.25 bits, of which 26 bits comprise a training sequence. The summation circuit 730 strips the training sequence from the input to the data slicer 728 and correlates the training sequence to the stored training sequence code 738. The result of this correlation is provided to the coefficient adaptation circuit 739 which iteratively sets the feedforward coefficients g_0, g_1, g_2, g_3...g_{n-1} and feedback DFE coefficients ϵ_0, ϵ_1, ϵ_2, ϵ_3...ϵ_m and compares the training sequence stripped from the resulting input to the data slicer 728 to the known training sequence code 738 until an optimum match is achieved.

The feedback filter 750, like the feedback filter 596 of Fig. 10, eliminates the postcursor portion of ISI, albeit in an adaptive manner. To this end, the feedback filter 750 includes a plurality of delay circuits 740_0, 740_1, 740_2, ...740_n, the outputs of which provide respective scale factor values α_{-1}, α_{-2}, α_{-3}, ...α_{-n}. The scale factors α_{-1}, α_{-2}, α_{-3}, ...α_{-n} are multiplied in multipliers 742_1, 742_2, 742_3, ...742_m by corresponding feedback coefficients ϵ_1, ϵ_2, ϵ_3, ...ϵ_m. The signals 744_1, 744_2, 744_3, ...744_m provided by multipliers 742_1,

742_2, 742_3, ...742_m are coupled to the summation circuit 724 where they are summed with output signals 714_0, 714_1, 714_2, ...714_{n-1} from the feedforward filter 710.

Referring also to Fig. 13, a flow diagram of steps performed by the signal processor of Fig. 12 is shown. It is noted that the steps associated with adaptive coefficient determination are omitted from Fig. 13 for simplicity. In step 800, the signal processor 35 waits for an interrupt IRQ2 which is generated by the $\overline{DA}$ output signal 406 of the P/D converter 260. In step 804, a timer is read to determine the time ET_2 that has lapsed since a prior IRQ2 interrupt was received. The time ET_2 is stored and the timer is loaded with a count of 100 and restarted.

In step 808, the current difference value d(x) is stored as the previous difference value $d(x)_{-1}$. Thereafter, the current count value signal 264 from the P/D converter 260 is stored as a value N. A new difference value is then computed in step 816 by subtracting 246 from the value N. An intermediate integrator value f(x)' is then computed in step 820 by multiplying the previous difference value $d(x)_{-1}$ by the timer value ET_2. In a subsequent step 824, the intermediate integrator value f(x)' is incremented by the previous intermediate integrator value $f(x)'_{-1}$. In step 828, the current intermediate integrator value f(x)' is set to the previous intermediate integrator value $f(x)'_{-1}$. The Mask Off IRQ0 box 832 indicates sequential steps 804 through 828 are completed once the sequence is entered.

In a subsequent step 836, the signal processor 35 idles, after which it waits for an interrupt IRQ0, provided by the 270.833KHz recovered clock signal 482 (Fig. 8A). Once an IRQ0 interrupt is received, step 844 is next performed in which the timer is again read and the lapsed time since the last IRQ0 interrupt stored as timer value ET_0. The timer is also loaded with a value of 100 and restarted in step 844. In a step 848, a value I is set equal to the sum of the current integrator value f(x)' and the product of the difference

value d(x) and the timer value ET_0. Steps 816-848 collectively represent the operation of the integrator 702 of Fig. 12. Thereafter, the previous intermediate integrator value $f(x)'_{-1}$ is set to zero.

The operation of the feedforward filter 710 and summation circuit 724 is then performed in step 856, in which a value I′ is computed by summing the products of the delayed signals I_{n-1} 718_0, I_{-1} 718_1, ... I 718_{n-1} with the corresponding feedforward coefficient g_0, g_1, ... g_{n-1}. Note that in the illustrative flow diagram of Fig. 13, n=3. Thereafter, in a step 860, the operation of the feedback filter 750 and the summation circuit 724 is performed by computing a value I′′ which is equal to the summation of the value I′ and the product of each of the scale factors α_{-1}, α_{-2}, ...α_{-n} with the corresponding DFE constant ϵ_1, ϵ_2, ..ϵ_m. In the illustrative embodiment, the value m=2. The value I′′ represents the output signal of the summation circuit 724 provided to the data slicer 728 (Fig. 12).

The operation of the data slicer 728 is performed in steps 864 and 872. In particular, in step 864, if it is determined that the value I′′ is greater than or equal to zero, then the transmitted bit is a zero. In step 872, if it is determined that the value I′′ is less than zero, then the transmitted bit is a one.

The scale factor value α is then computed in steps 868 and 876. In particular, if the transmitted bit is a zero, then the scale factor value α is set to -1 in step 868. Alternatively, if the transmitted bit is a one, then the scale factor value α is set to +1 in step 876. Thereafter, in step 890, the data signal 462 (Fig. 8A) is provided to the one bit latch 458. The scale factor values α_{-1}, α_{-2}, ...α_{-n} are then computed in steps 894 and 896, for n=2. That is, in step 894, the α_{-2} scale factor value is set equal to the α_{-1} scale factor value and, in step 896, the α_{-1} scale factor value is set equal to the α scale factor value. The Mask Off

IRQ0 box 900 indicates that the sequence of steps 840 through 896 is completed once entered.

As noted above, the receiver 10 described herein is readily adaptable for use in receiving RF signals modulated by various analog and digital schemes. In particular, the required modifications to the receiver include modifying the bandwidth of the RF BPF 18, the down converter frequency (i.e., the frequency of the LO signals 60 and 62 in Fig. 2), the bandwidth of the IF LPF 30 and the demodulation technique employed by the signal processor 35.

Consider for example, modification of the receiver 10 to process received RF signals which are analog FM modulated in the FM broadcast band. In this case, the bandwidth of the RF BPF 18 is changed from between 935MHz and 960MHz to between 88MHz and 108MHz. The frequency of the down conversion LO signals 60, 62 is reduced from between 935.2MHz and 959.8MHz to between 88MHz and 108MHz, depending on the channel of interest, and the IF bandwidth remains unchanged at 200KHz. In processing FM signals, the demodulation performed by the signal processor 35 generates a complex signal. A conventional stereo decoder is used to decode L and R channels.

Having described the preferred embodiments of the invention, it will now become apparent to one of skill in the art that other embodiments incorporating their concepts may be used. It is felt therefore that these embodiments should not be limited to disclosed embodiments but rather should be limited only by the spirit and scope of the appended claims.

CLAIMS

1. An RF receiver comprising:

a down converter for converting a received RF signal to in-phase and quadrature zero IF signals;

a channel selection filter for passing a selected frequency component of said in-phase and quadrature zero IF signals; and

an up converter for converting said selected frequency component of said in-phase and quadrature zero IF signals to an IF signal.

2. The RF receiver recited in claim 1 wherein said channel selection filter comprises an in-phase active filter and a quadrature active filter.

3. The RF receiver recited in claim 1 wherein said down converter is an image reject filter.

4. The RF receiver recited in claim 1 wherein said up converter is an image canceling filter.

5. The RF receiver recited in claim 1 further comprising an amplifier for providing gain to said IF signal.

6. The RF receiver recited in claim 5 further comprising a phase comparator responsive to said IF signal for providing a zero crossing signal indicative of zero crossings of said IF signal.

7. The RF receiver recited in claim 6 further comprising a quantizer for quantizing said zero crossing signal.

8. The RF receiver recited in claim 7 wherein said quantizer comprises a period-to-digital converter responsive

to said zero crossing signal for providing a count signal representative of the period between consecutive zero crossings of said IF signal and the instantaneous frequency of said IF signal.

9. The RF receiver recited in claim 8 further comprising a signal processor for processing said count signal.

10. The RF receiver recited in claim 9 wherein said signal processor comprises:

a demodulator for demodulating said count signal; and

an equalizer for removing the effects of intersymbol interference on said count signal.

11. The RF receiver recited in claim 10 wherein said signal processor further comprises a second equalizer for removing the effects of time dispersion on said count signal.

12. The RF receiver recited in claim 11 wherein said signal processor is a digital signal processor.

13. A method for processing a received RF signal comprising the steps of:

converting said RF signal to in-phase and quadrature zero IF signals;

passing a selected frequency component of said in-phase and quadrature zero IF signals; and

converting said passed frequency selected component of said in-phase and quadrature zero IF signals to an IF signal.

14. The method recited in claim 13 further comprising the step of providing gain to said IF signal.

15. The method recited in claim 13 further comprising the step of comparing said IF signal to a reference signal to

provide a zero crossing signal indicative of zero crossings of said IF signal.

16. The method recited in claim 15 further comprising the step of quantizing said zero crossing signal to provide a count signal representative of the period between consecutive zero crossings of said IF signal and the instantaneous frequency of said IF signal.

17. The method recited in claim 16 further comprising the steps of:

equalizing said count signal to remove the effect of intersymbol interference on said count signal; and

demodulating said count signal.

18. A RF receiver comprising:

a converter and filter for converting a received RF signal to an IF signal having a selected frequency component;

a phase comparator for comparing said IF signal to a reference signal to provide an amplitude limited output signal indicative of zero crossings of said IF signal; and

a quantizer for quantizing said output signal of said phase comparator so as to provide a count signal representative of the period between consecutive zero crossings of said IF signal and the instantaneous frequency of said IF signal.

19. The RF receiver recited in claim 18 wherein said converter and filter comprises:

a down converter for converting said received RF signal to in-phase and quadrature zero IF signals;

a channel selection filter for passing said selected frequency component of said in-phase and quadrature zero IF signals; and

an up converter for converting said selected frequency component of said in-phase and quadrature zero IF signals to an IF signal.

20. The RF receiver recited in claim 18 further comprising a signal processor for demodulating and equalizing said count signal.

21. An RF receiver receiving a transmitted RF signal modulated in accordance with a predetermined modulation scheme, said RF receiver comprising:

an RF bandpass filter for filtering said received RF signals to pass RF signals within a predetermined frequency band;

a down converter for converting an RF signals within said predetermined frequency band to in-phase and quadrature zero IF signals, said down converter comprising a mixer for mixing said RF signals within said predetermined frequency band with a local oscillator signal having a first local oscillator frequency;

a channel selection filter responsive to said in-phase and quadrature zero IF signals for passing a selected frequency component of said in-phase and quadrature zero IF signals;

an up converter for converting said selected frequency component of said in-phase and quadrature zero IF signals to an IF signal having an IF frequency, said up converter comprising a mixer for mixing said selected frequency component of said in-phase and quadrature zero IF signals with a local oscillator signal having a second local oscillator frequency;

a quantizer for quantizing said IF signal to provide a count signal indicative of the period between consecutive zero crossings of said IF signal; and

a demodulator for demodulating said count signal in accordance with a demodulation technique in order to recover

said transmitted RF signal, wherein said predetermined frequency band, said first local oscillator frequency, IF frequency and said demodulation technique are selectable in accordance with said predetermined modulation scheme of said RF signals.

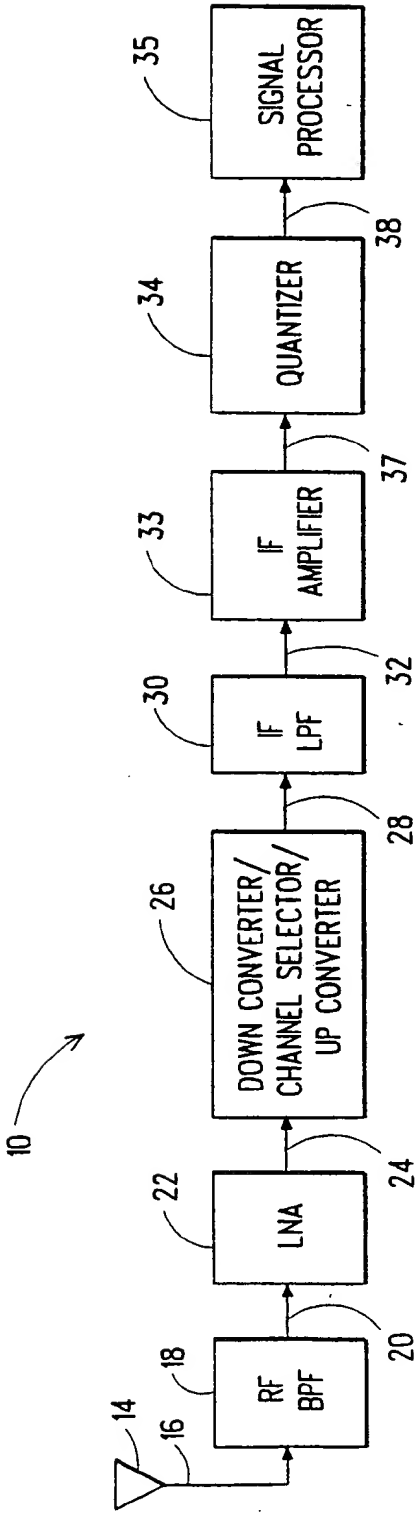

FIG. 1

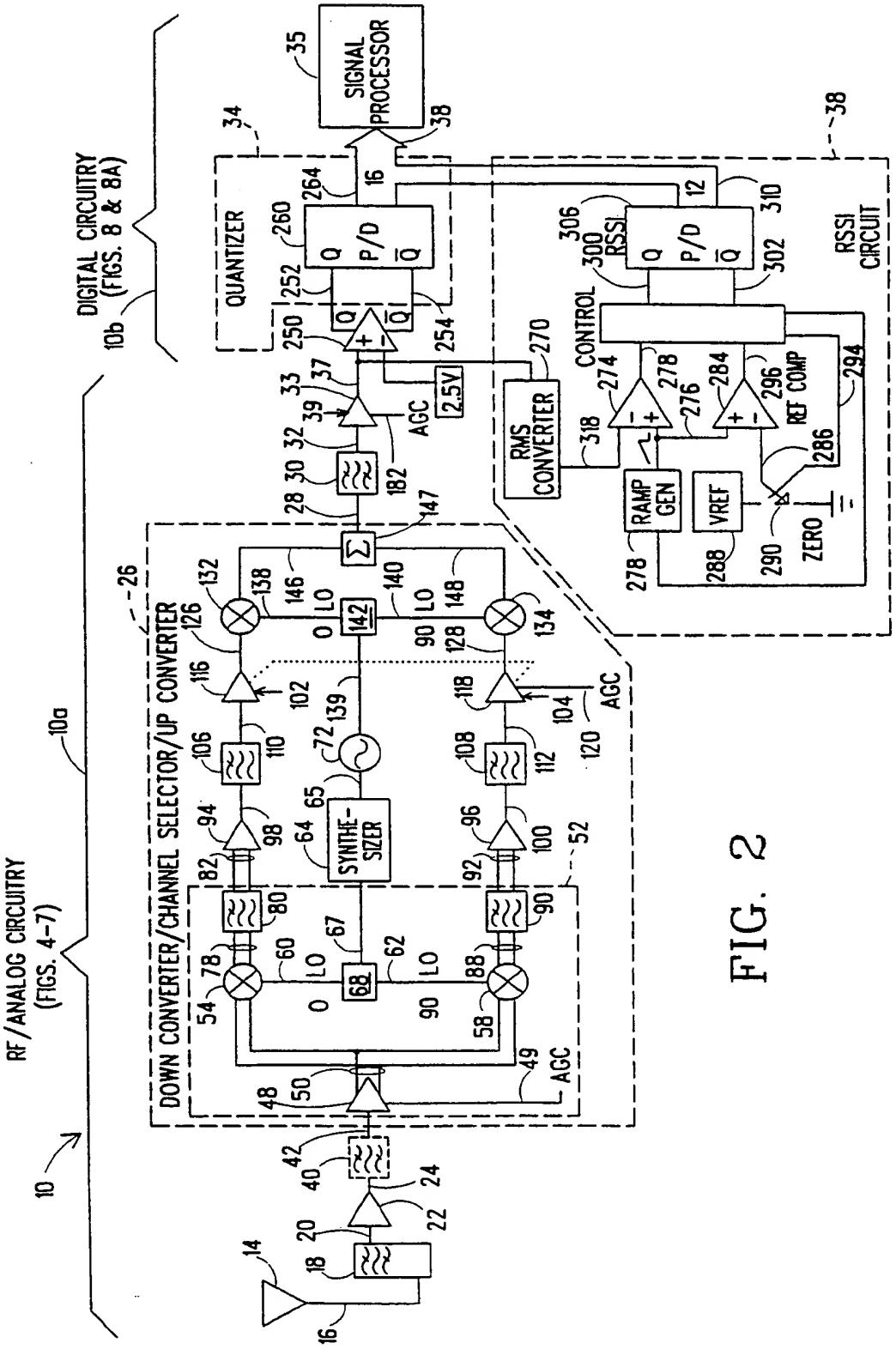

FIG. 2

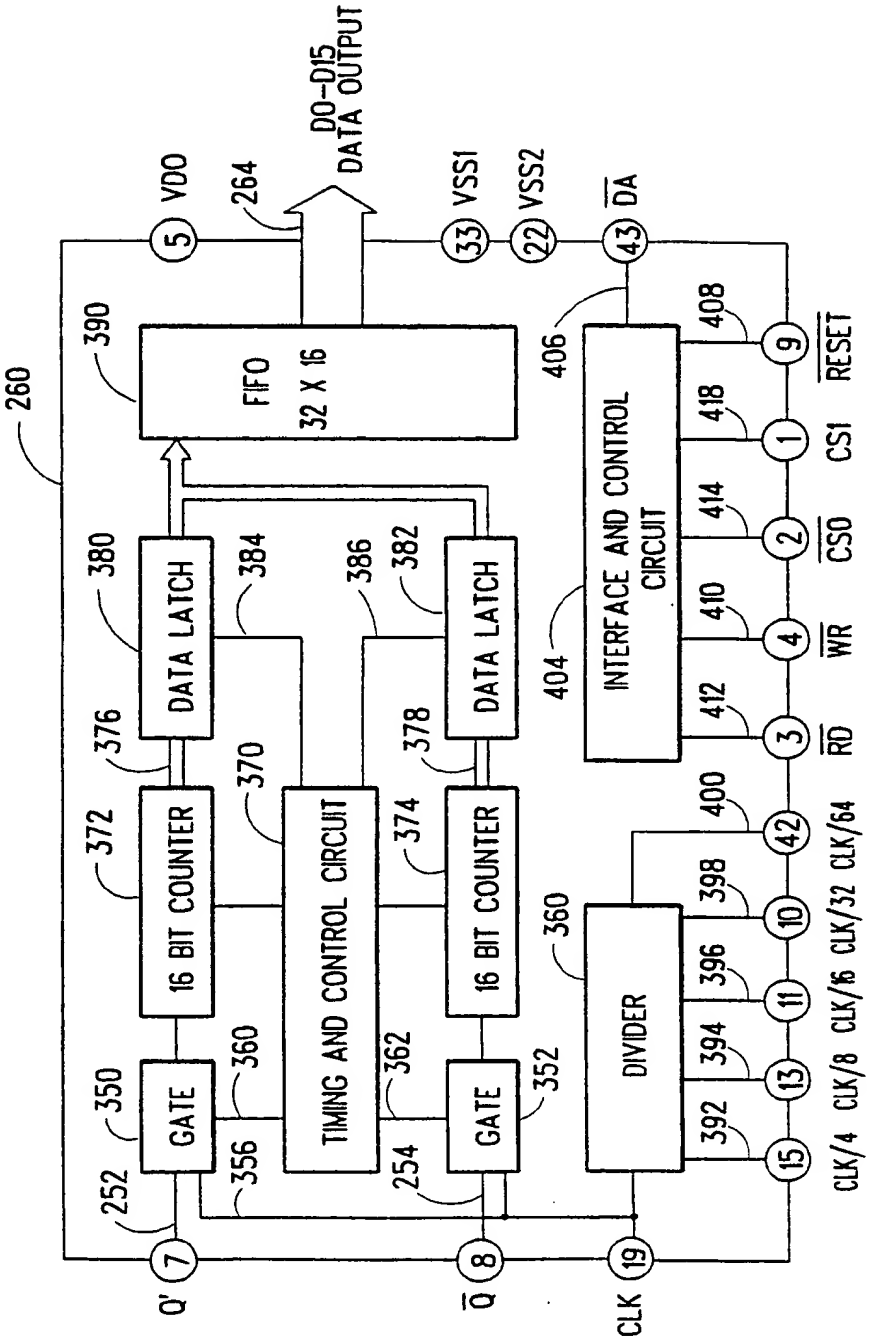

FIG. 3

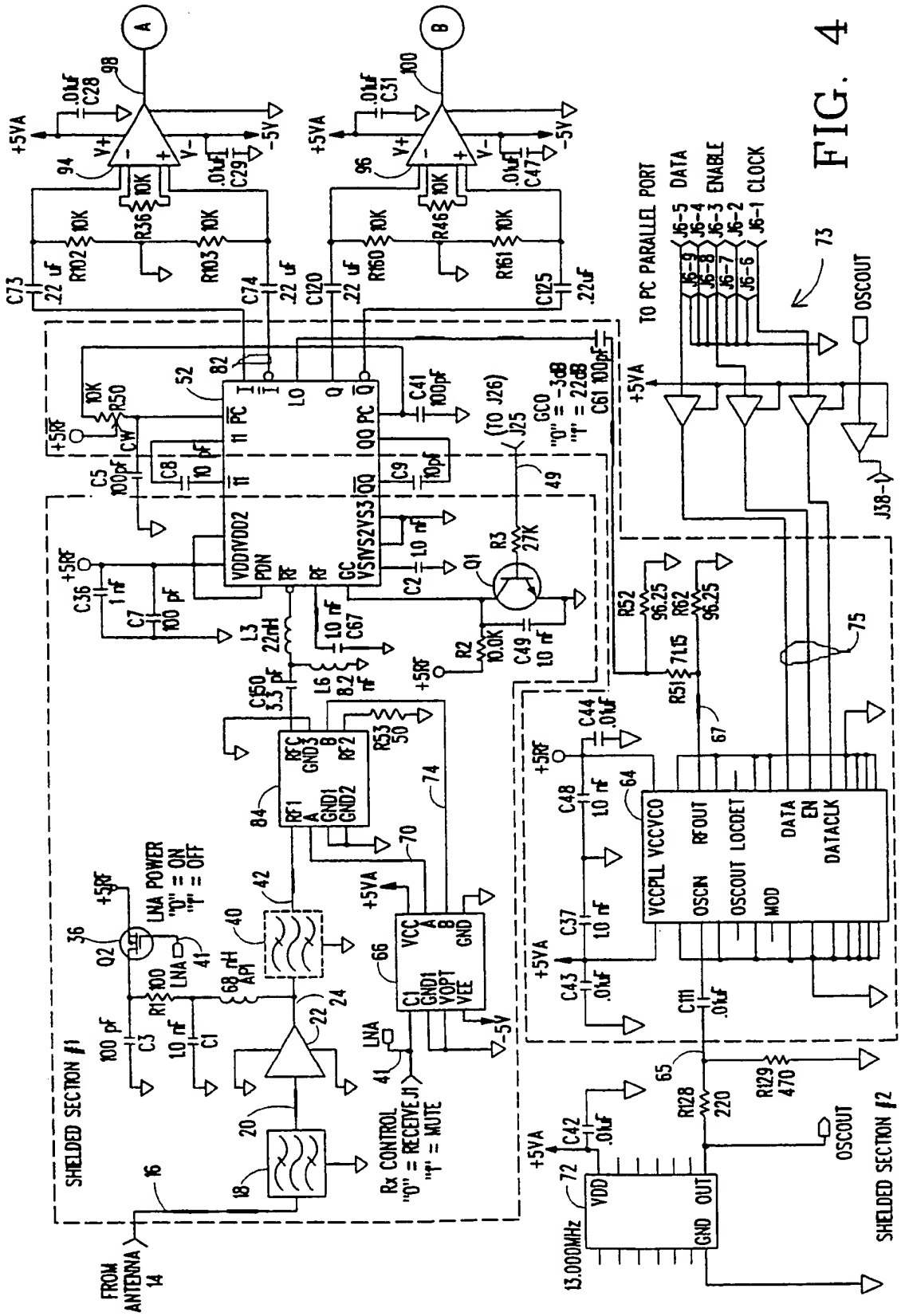

FIG. 4

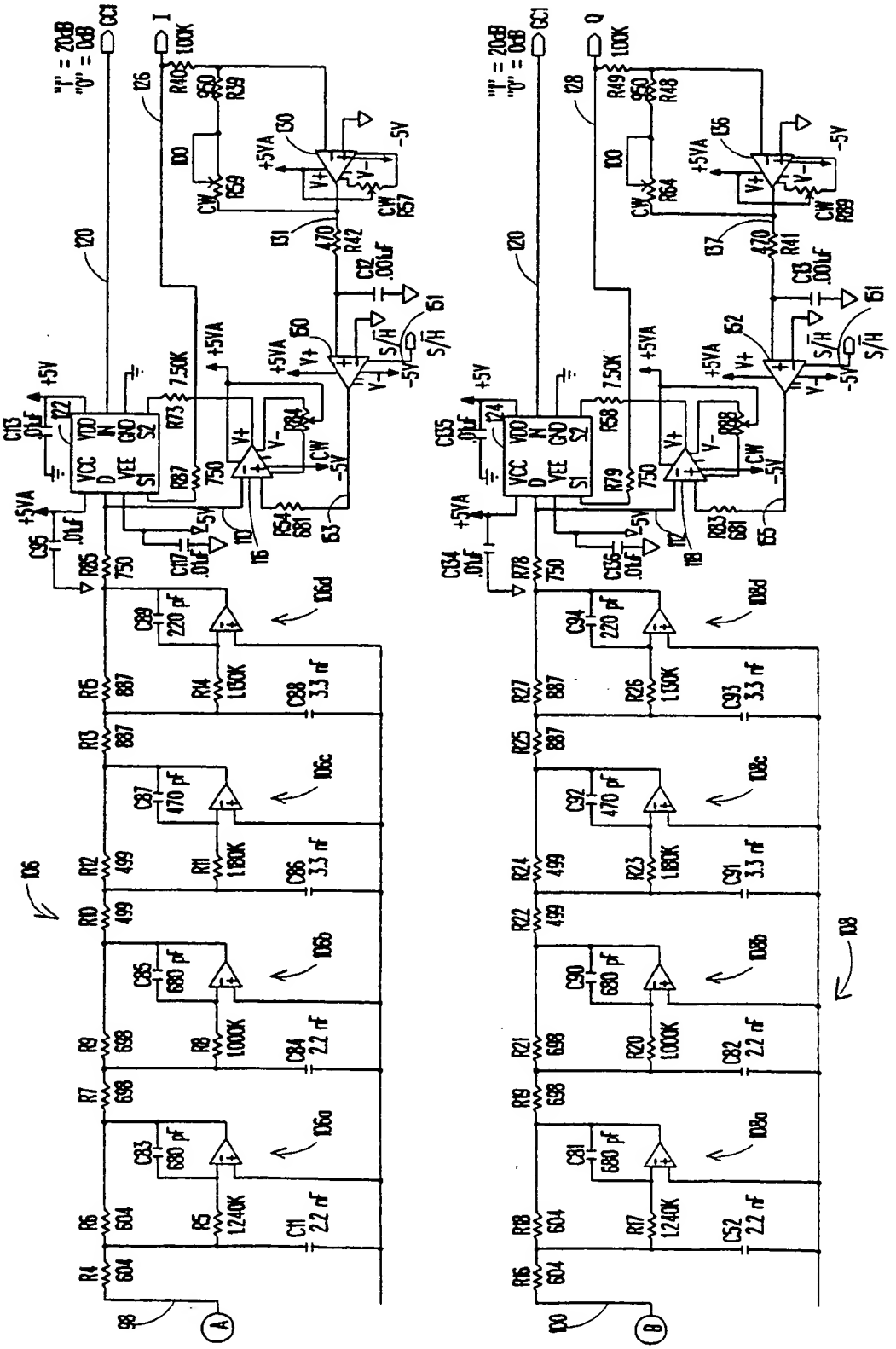

FIG. 5

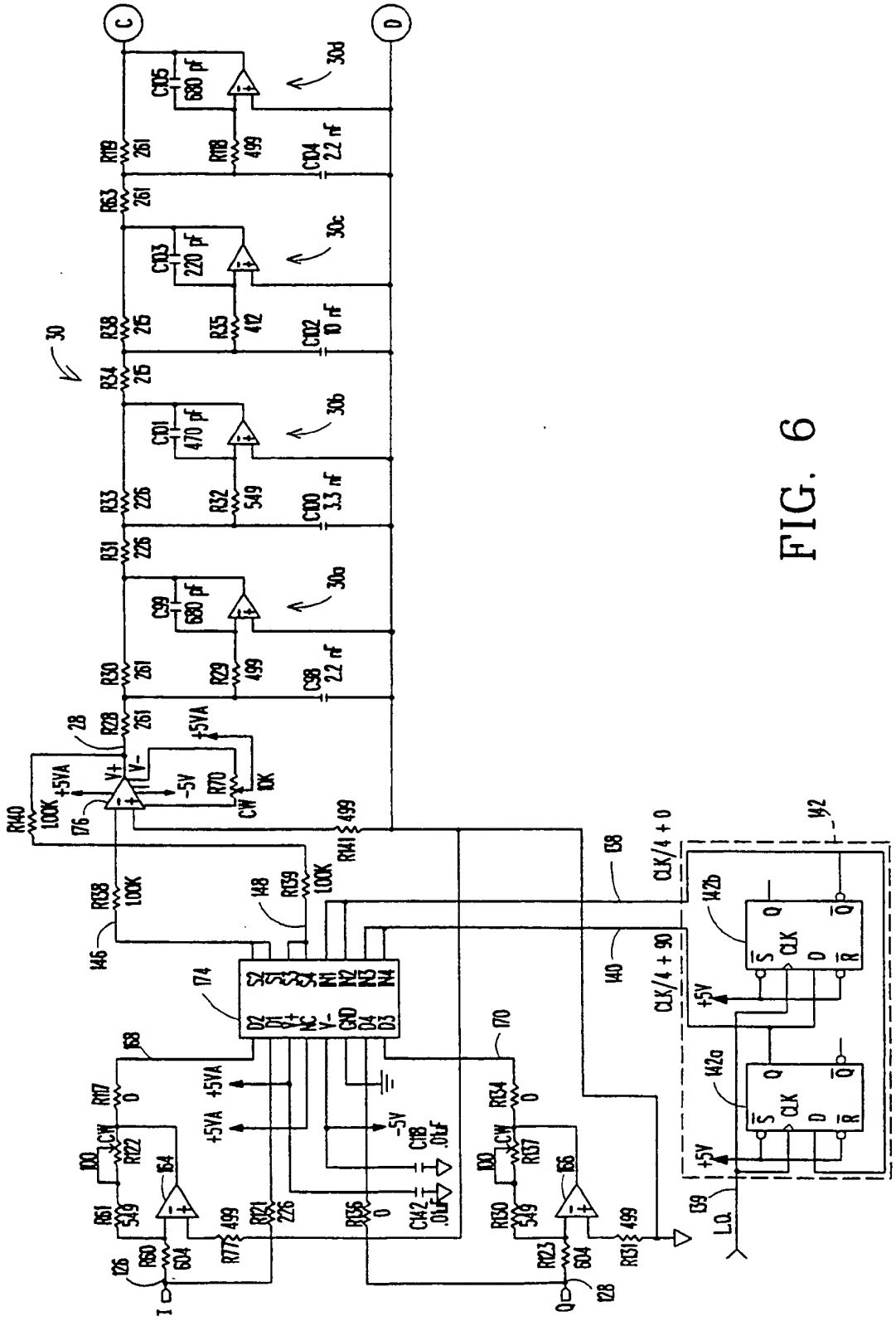

FIG. 6

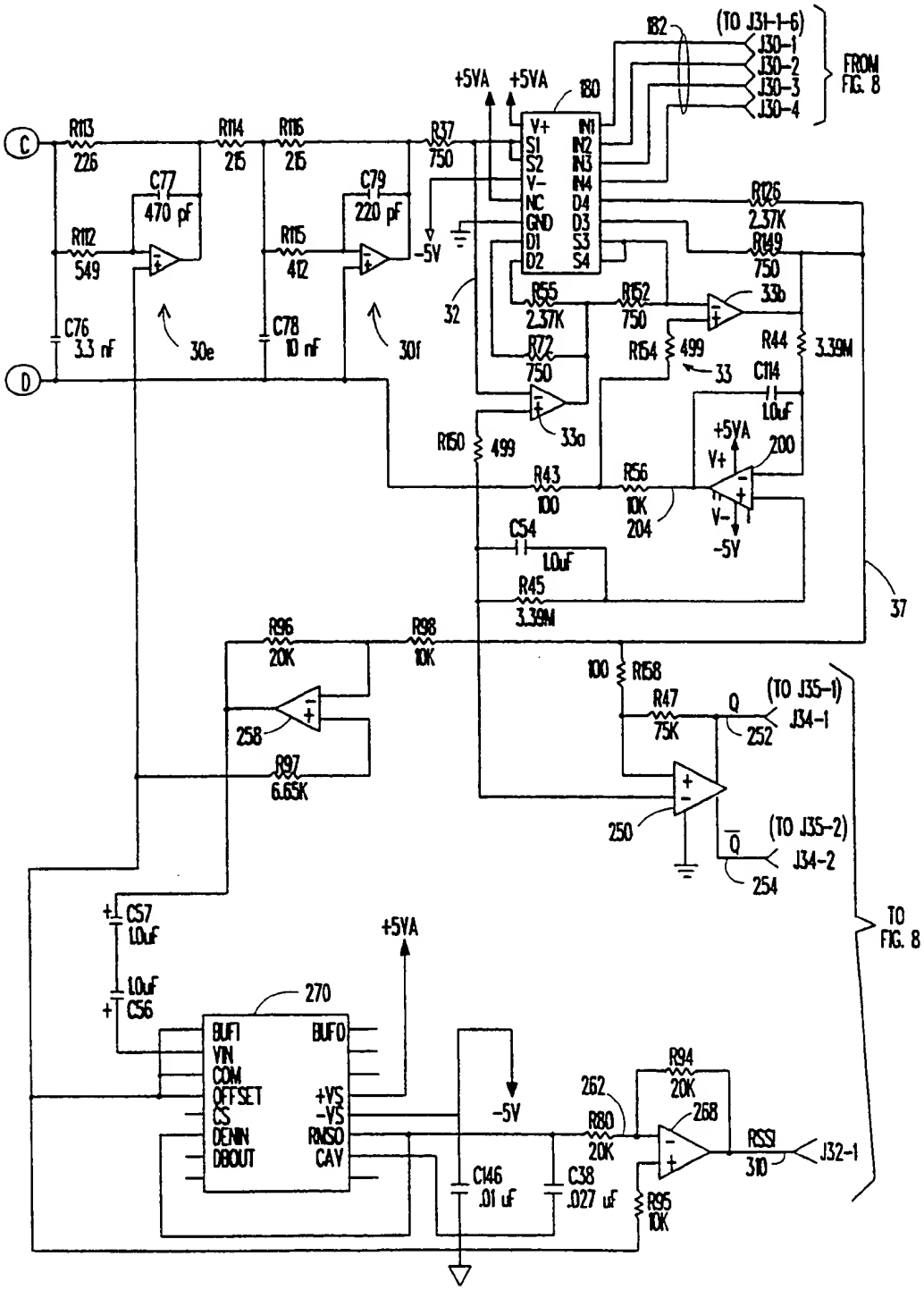

FIG. 7

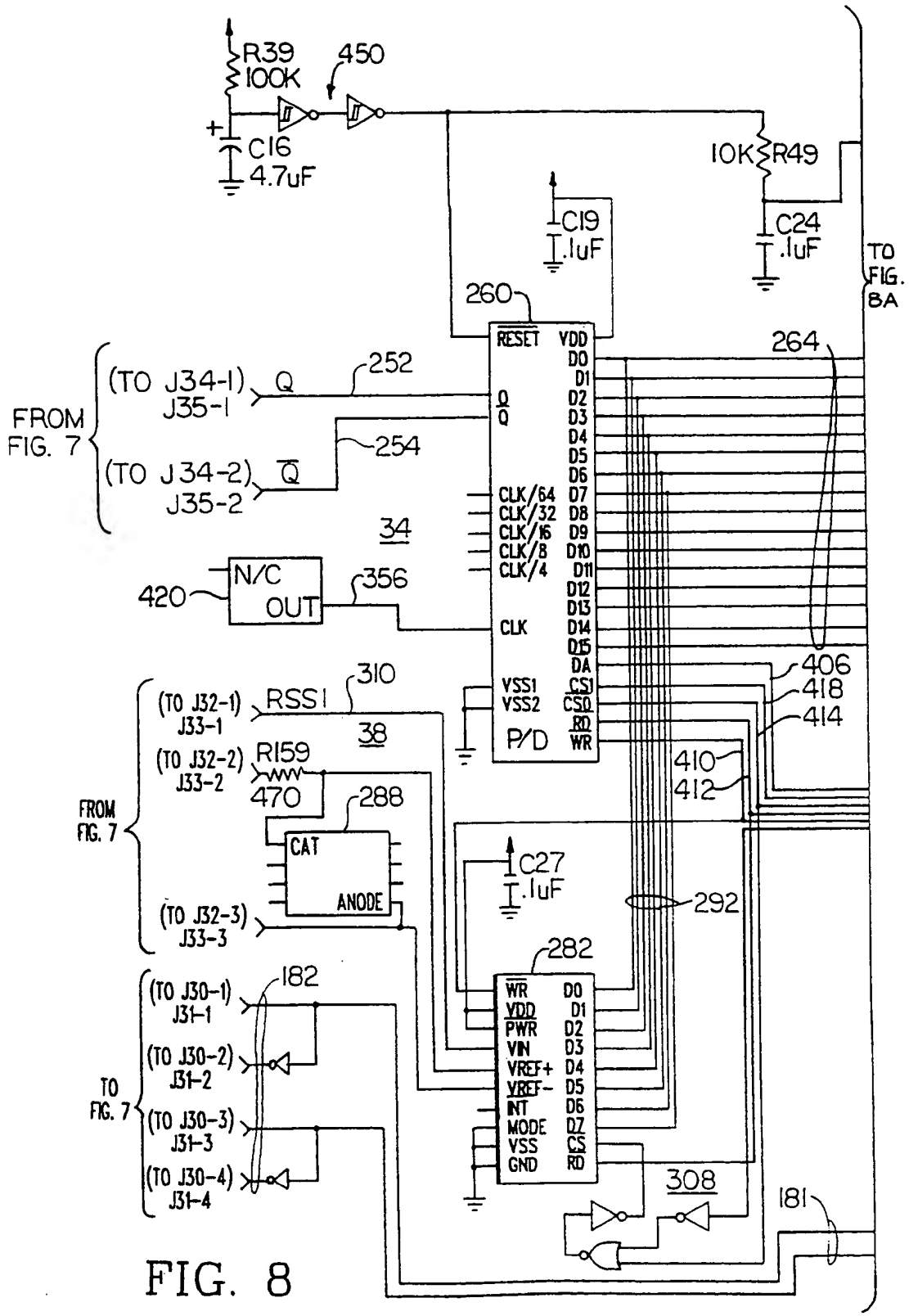

FIG. 8

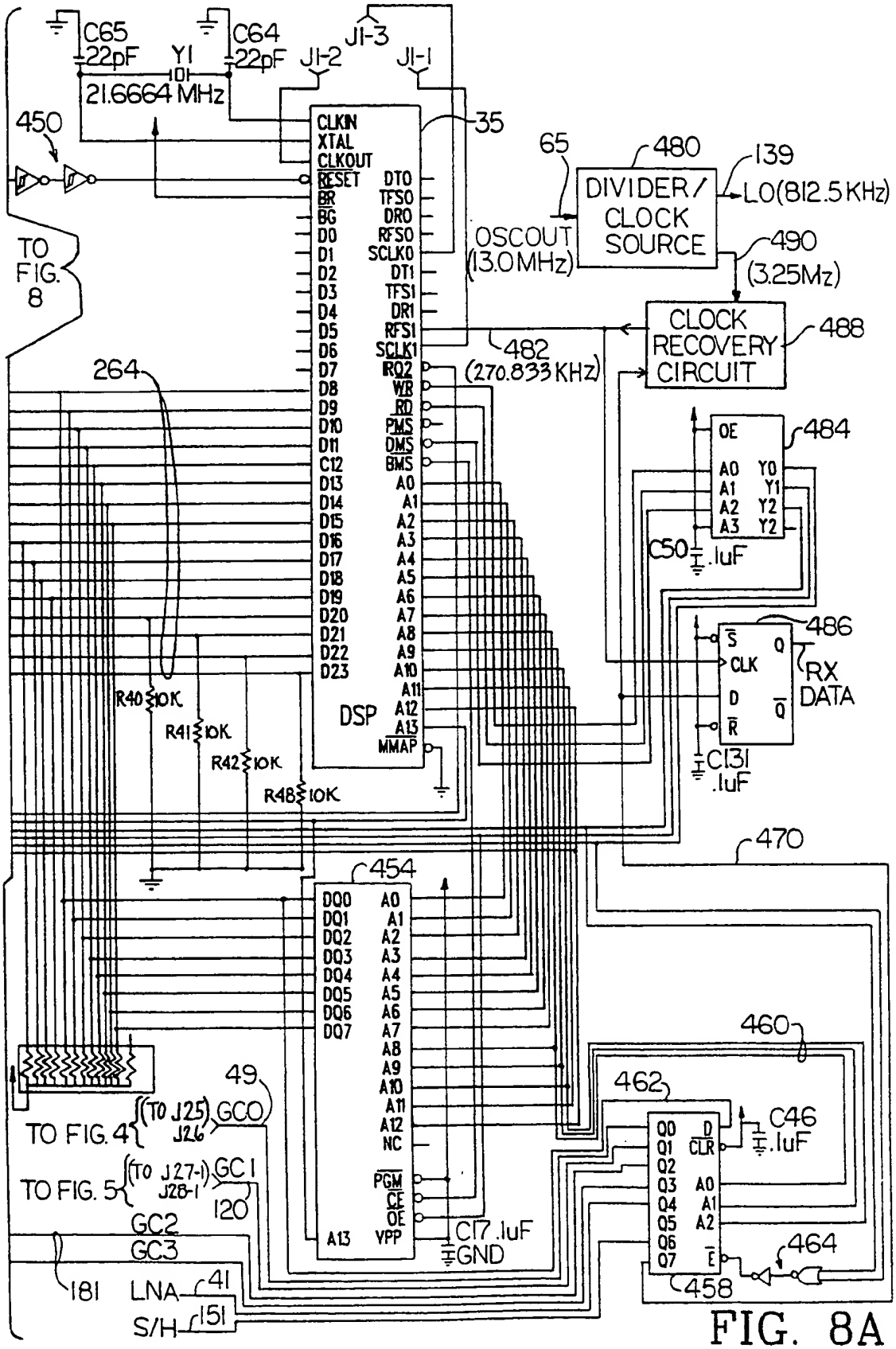

FIG. 8A

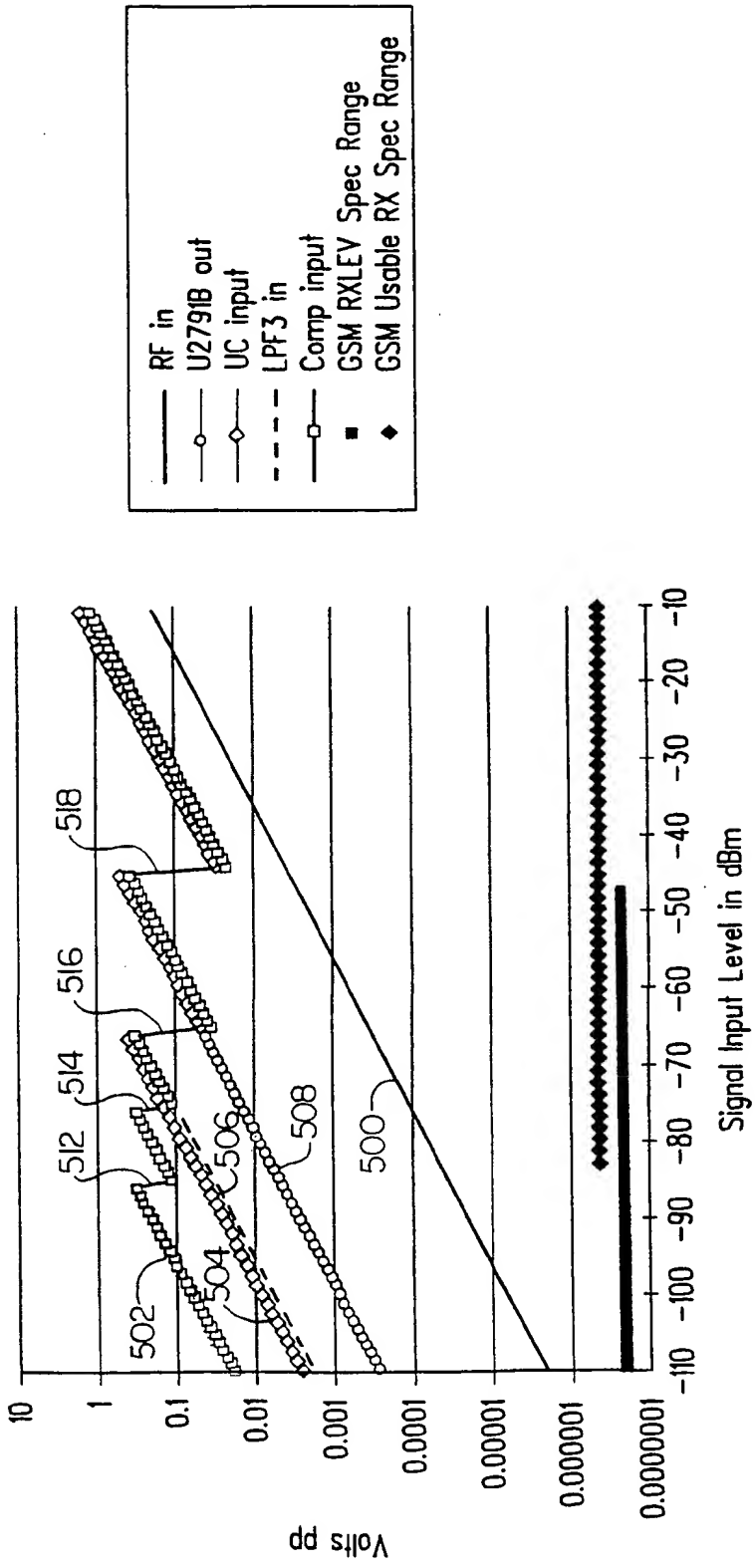

FIG. 9

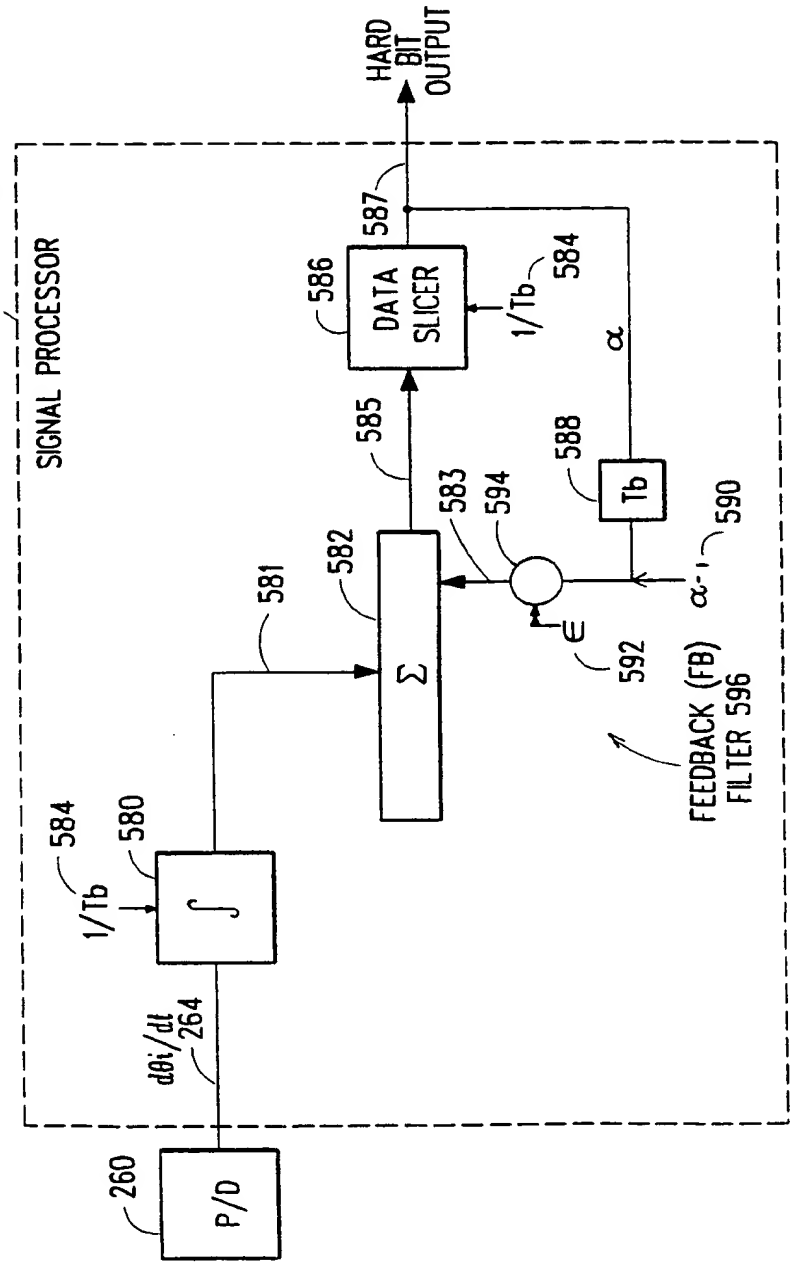

FIG. 10

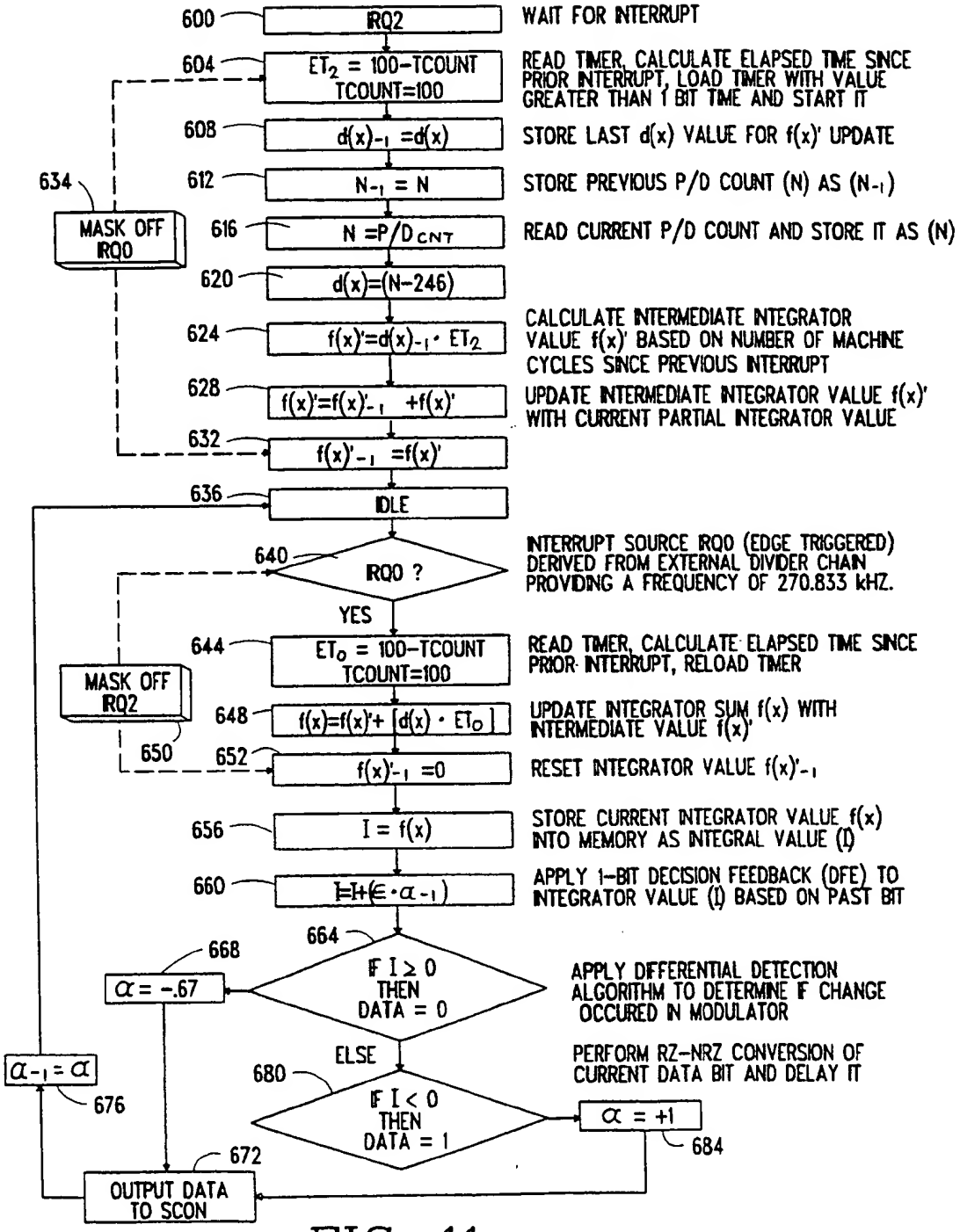

FIG. 11

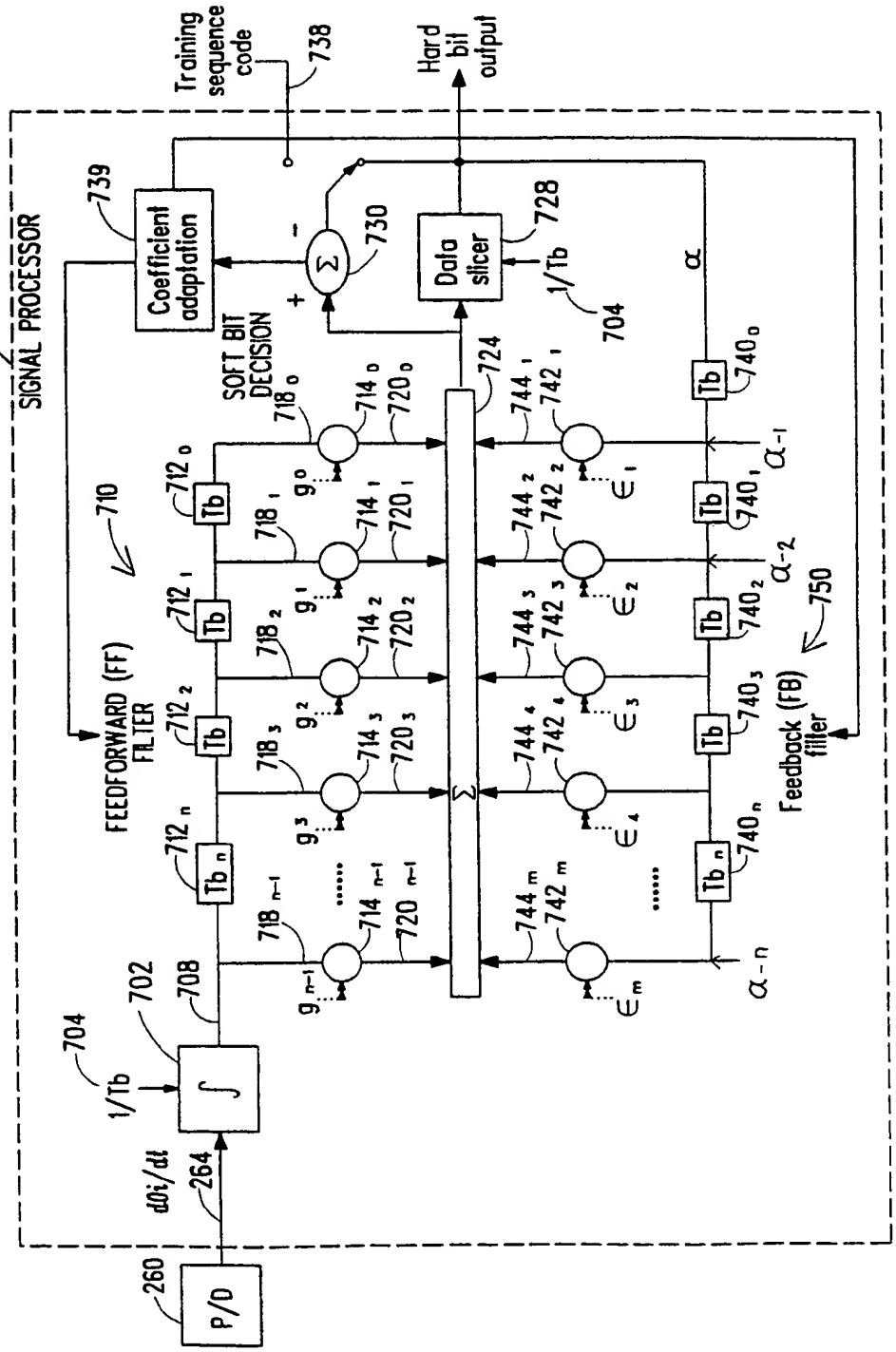

FIG. 12

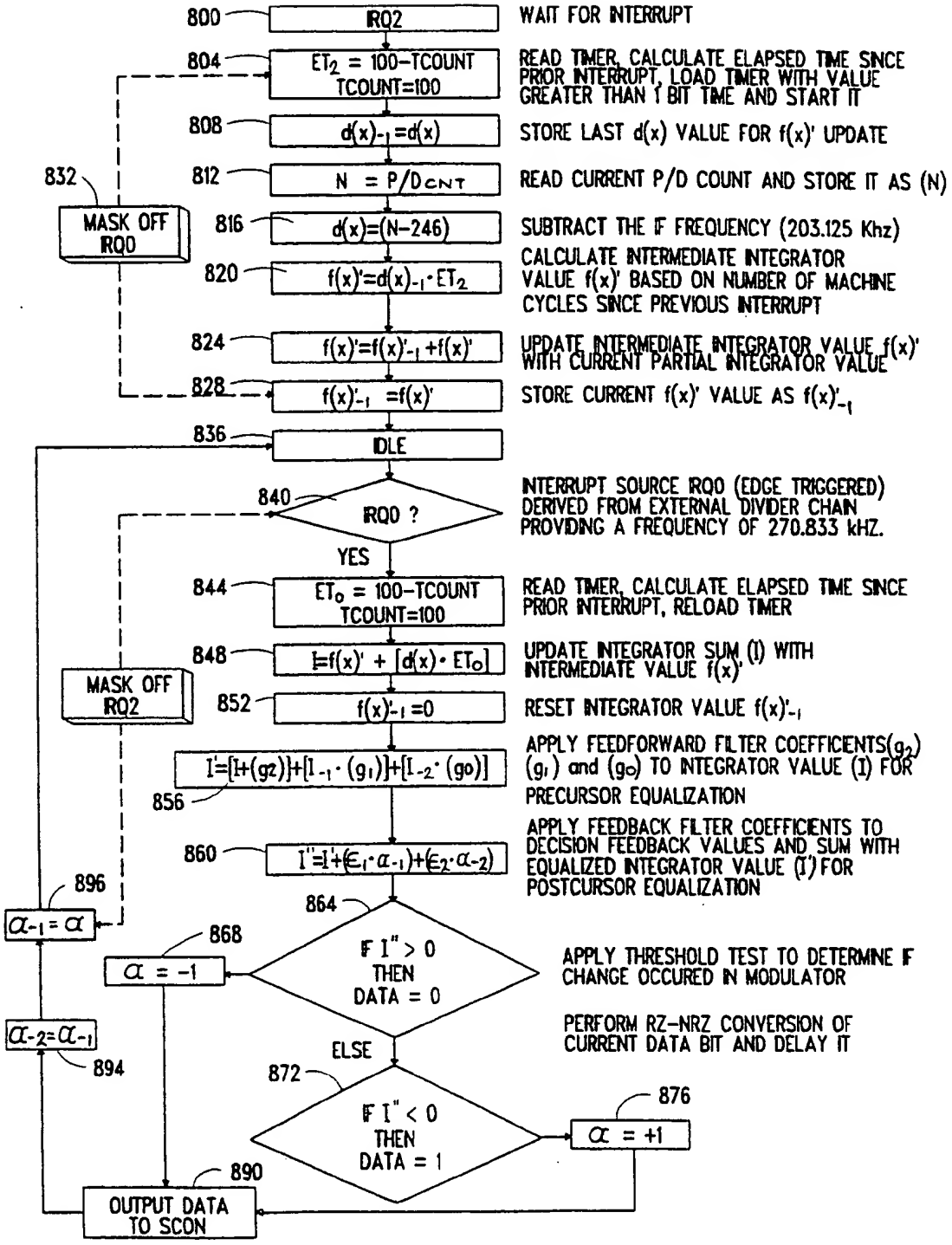

FIG. 13

INTERNATIONAL SEARCH REPORT

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PCT/US96/12727

A. CLASSIFICATION OF SUBJECT MATTER

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US CL :455/207, 303, 306, 314

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/207, 296, 303, 306, 307, 314; 375/330, 349

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,323,391 (Harrison) 21 June 1994, see entire document.	1-21
A	US, A, 5,355,533 (Dickerson) 11 October 1994, see entire document.	1-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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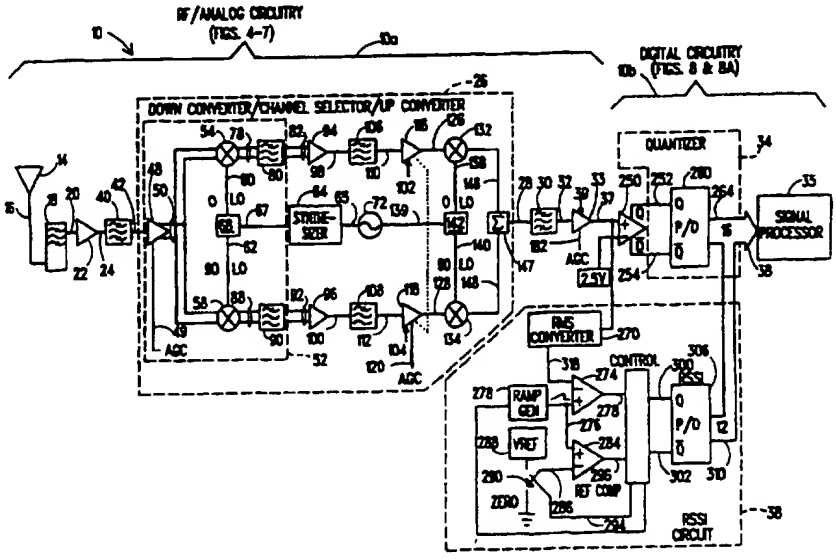
Published
With international search report.

(54) Title: UNIVERSAL RF RECEIVER



(57) Abstract

A universal receiver (10) for processing RF signals modulated by various analog and digital modulation techniques. The receiver (10) includes a down converter (52) for converting received RF signals to in-phase and quadrature zero IF signals, and active low pass filter (106, 108) for channel selection and an up converter (132, 134) for converting the channel selected in-phase and quadrature zero IF signals to an IF signal. Only moderate system gain is introduced at zero IF in order to avoid increasing any DC offsets. The receiver (10) further includes DC offset compensation circuitry and a period-to-digital (P/D) converter (260) for quantizing the IF signal. A signal processor (35) equalizes and demodulates the IF signal to recover the transmitted signal.

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